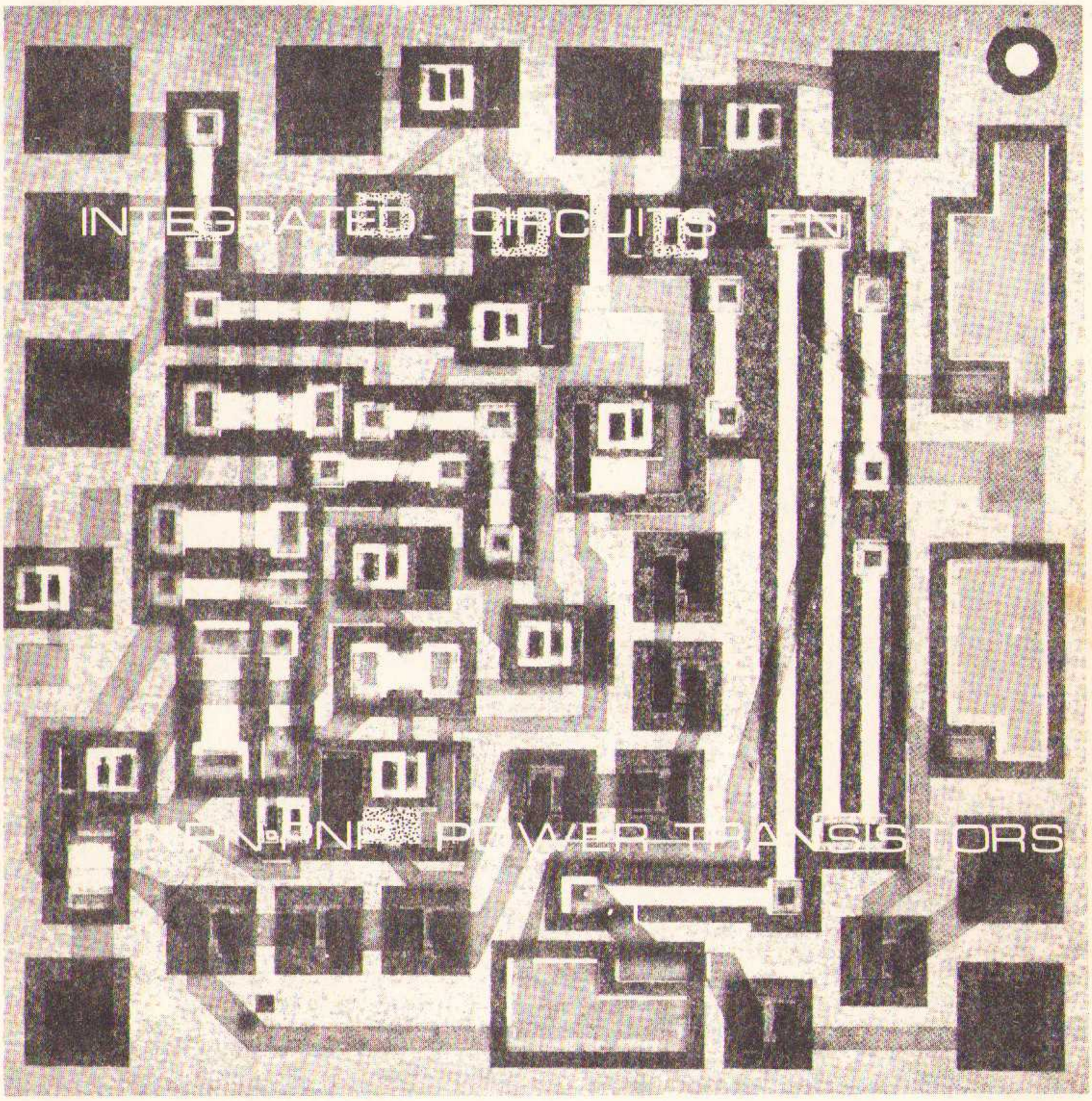
TECHNISCHE DOCUMENTATIE 1969
DEEL 7•8 ——— JULI •AUG.



PRIJS *f* 3,50

Technische documentatie 1969, tweede jaargang, juli-augustus 1969

Abonnementsprijs per jaar *f* 10,40 incl. 4% B.T.W.

Omslagfoto: geïntegreerde schakeling, schijfje silicium met een complete versterker, ware grootte circa 1 mm^2.

Verhuizingen:
Bij verhuizing danwel onjuiste adressering dient hiervan vóór de eerste van de maand onze administratie op de hoogte worden gesteld. Hierbij dient het bij de adressering opgenomen nummer te worden vermeld; zonder dit nummer kunnen adreswijzigingen beslist niet in behandeling worden genomen. Correspondentie te richten aan: Van Dam Elektronica, afd. T.D. 1969, Postbus 3149 te Rotterdam-noord.

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Voor onze leveringsvoorwaarden zie Technische Documentatie deel 1, blz. 2.
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Inleiding bij deel 7 en deel 8.

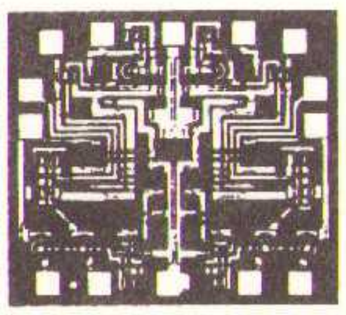
In deze uitgave wordt, evenals in deel 5 en deel 6, voor een groot gedeelte aandacht besteed aan de volledige technische gegevens van interessante produkten. Deze gegevens zijn voor vele amateurs en laboratoria van groot nut gebleken voor het samenstellen van zéér interessante elektronische schakelingen met moderne halfgeleiders. Vooral de nieuwste N.P.N./P.N.P. power transistoren van Texas Instuments hebben grote belangstelling bij de HIFI-liefhebbers ondervonden. In de komende nummers hopen wij enkele schakelingen op te nemen, welke wij met deze produkten hebben ontwikkeld. Ook aan onze lezers willen wij gaarne de mogelijkheid openstellen, hun schakelingen aan anderen door te geven; hiertoe stellen wij gaarne ruimte ter beschikking. In dat geval stellen wij het op prijs aan het prototype enkele laboratorium-metingen te mogen verrichten, teneinde de specificaties en het reproduceerbaarheidspercentage te kunnen bepalen en eventueel te verbeteren.

★ TOT SLOT WIJZEN WIJ U ER MET GROTE NADRUK OP, DAT ZOWEL UW CORRESPONDENTIE ALS UW POSTORDERS DIENEN TE WORDEN GESTUURD AAN ONS POSTBUS - ADRES:

Van Dam Elektronica, Postbus 3149 te Rotterdam-noord*

DIT VOORKOMT ONNODIGE VERTRAGING IN DE BEHANDELING TEN GEVOLGE VAN DE EEN MAAL PER DAG PLAATSHEBBENDE POSTBESTELLING !!!!!!!!

*Telefonische orders en inlichtingen: 010-240812-243497, administratie: 010-245516



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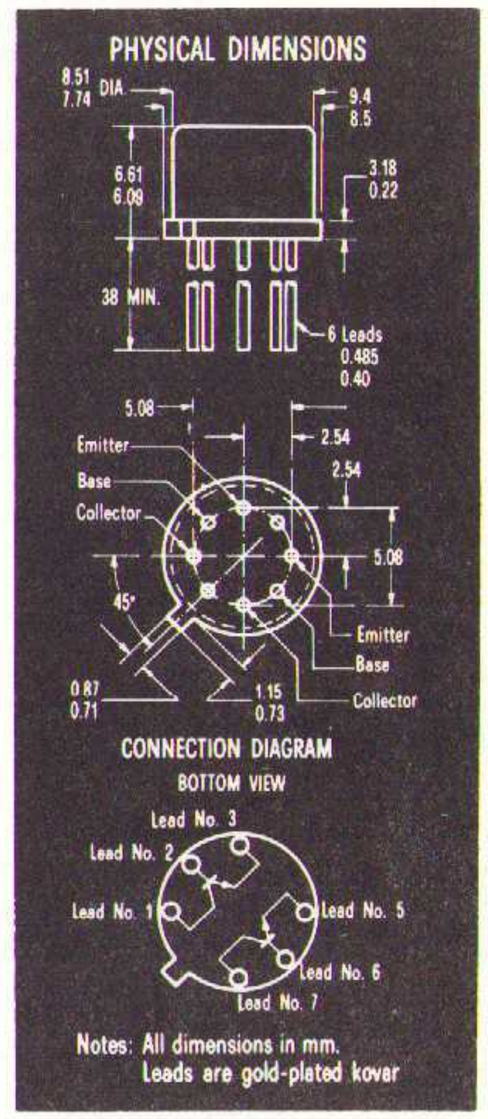
2C415

NPN DUAL, LOW·LEVEL, LOW·NOISE TRANSISTOR

GENERAL DESCRIPTION - The 2C415 is a six terminal device containing two isolated high gain, low noise NPN double diffused silicon PLANAR transistors in a hermetically sealed enclosure. It is designed for use in high performance differential amplifier circuits.



ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature	-55°C to + 175°C
Operating Junction Temperature	175°C Maximum
Lead Temperature (Soldering, 10 sec. time limit)	260°C Maximum

Maximum Power Dissipations

	One Side	Both Sides
Total Dissipation at 25°C Case Temperature (Notes 2 and 3)	0.68 Watt	1.1 Watt
at 100°C Case Temperature (Notes 2 and 3)	0.34 Watt	0.56 Watt
at 25°C Ambient Temperature (Notes 2 and 3)	0.34 Watt	0.43 Watt

Maximum Voltages and Current

BV_{CBO}	Collector to Base Voltage	45 Volts
LV_{CEO}	Collector to Emitter Voltage (Note 4)	35 Volts
BV_{EBO}	Emitter to Base Voltage	6.0 Volts
I_C	Collector Current Voltage	30 mA

ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
h_{FE}	DC Current Gain	60				I_C = 10 µA	V_{CE} = 5.0 V
h_{FE}	DC Current Gain	100	250			I_C = 100 µA	V_{CE} = 5.0 V
h_{FE}	DC Current Gain	150				I_C = 1.0 mA	V_{CE} = 5.0 V
V_{BE} (on)	Emitter to Base On Voltage			0.7	V	I_C = 0.1 mA	V_{CE} = 5.0 V
V_{CE} (sat)	Collector Saturation Voltage			0.4	V	I_C = 1.0 mA	I_B = 0.1 mA
BV_{CBO}	Collector to Base Breakdown Voltage	45			V	I_C = 10 µA	I_E = 0
BV_{EBO}	Emitter to Base Breakdown Voltage	6.0			V	I_E = 10 µA	I_C = 0
V_{CEO} (sust)	Collector to Emitter Sustaining Voltage (Notes 4 and 5)	35			V	I_C = 10 mA	I_B = 0
I_{CBO}	Collector Cutoff Current		3	10	nA	I_E = 0	V_{CB} = 40 V
I_{CBO} (150°C)	Collector Cutoff Current			10	µA	I_E = 0	V_{CB} = 40 V
I_{CEO}	Collector to Emitter Cutoff Current			10	nA	I_B = 0	V_{CE} = 5.0 V
I_{EBO}	Emitter Cutoff Current			10	nA	I_C = 0	V_{EB} = 5.0 V
h_{fe}	High Frequency Current Gain (f = 100 Mc/s)		1.0			I_C = 5.0 mA	V_{CE} = 5.0 V
C_{ob}	Output Capacitance			6.0	pF	I_E = 0	V_{CB} = 5.0 V
NF	Narrow Band Noise Figure (Note 6)			5.0	db	I_C = 10 µA	V_{CE} = 5.0 V
NF	Wide Band Noise Figure (Note 7)			5.0	db	I_C = 10 µA	V_{CE} = 5.0 V

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 175°C junction to case thermal resistance of 218°C/W for one side and 134°C/W for both sides.

(4) Rating refers to a high current point where collector-to-emitter voltage is lowest. For more information send for SGS-Fairchild AR5.

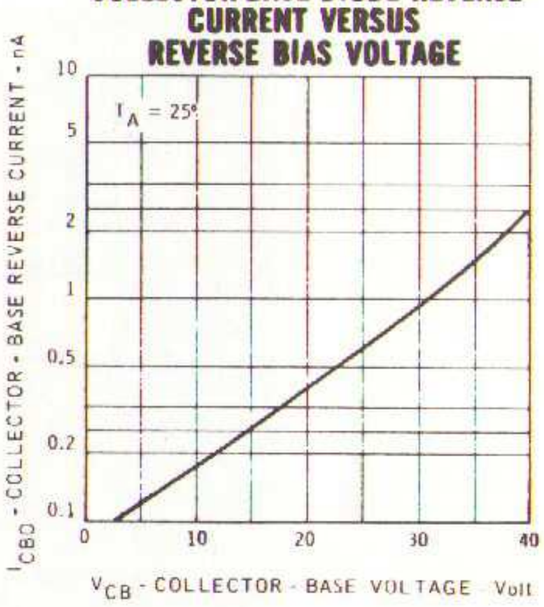
(5) Pulse Conditions: length = 300 µsec; duty cycle = 1%.

(6) Frequency = 1000 cps; 200 cycle-power bandwidth.

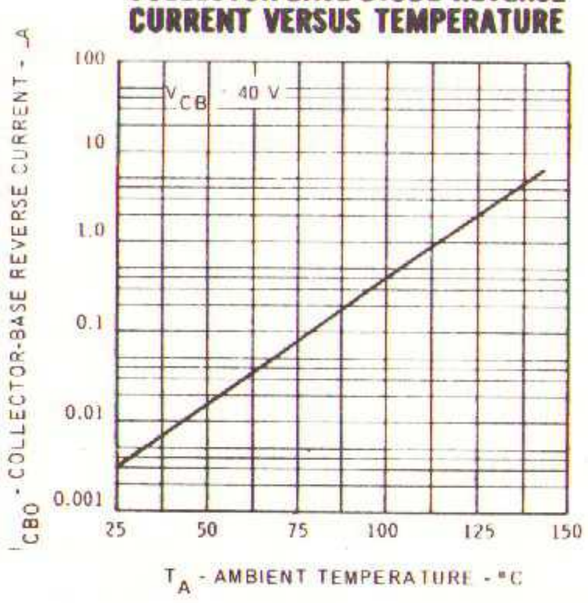
(7) The amplifier used for this measurement has a power bandwidth of 15.7 Kc/s and a response which rolls off 6 db per octave where the 3 db points are approximately at 25 cps and 10 Kc/s - R_G = 10 KΩ.

TYPICAL ELECTRICAL CHARACTERISTICS

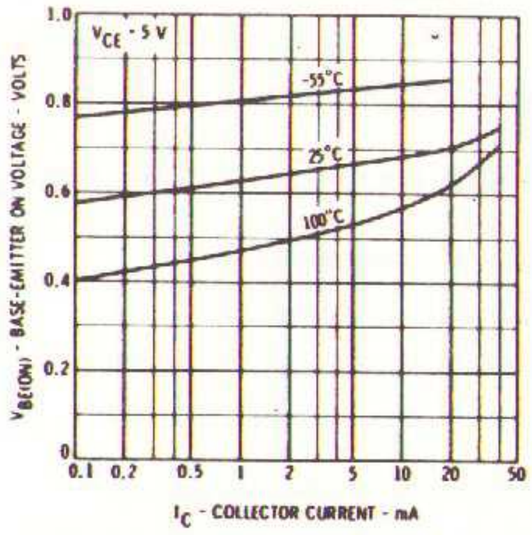
COLLECTOR-BASE DIODE REVERSE CURRENT VERSUS REVERSE BIAS VOLTAGE



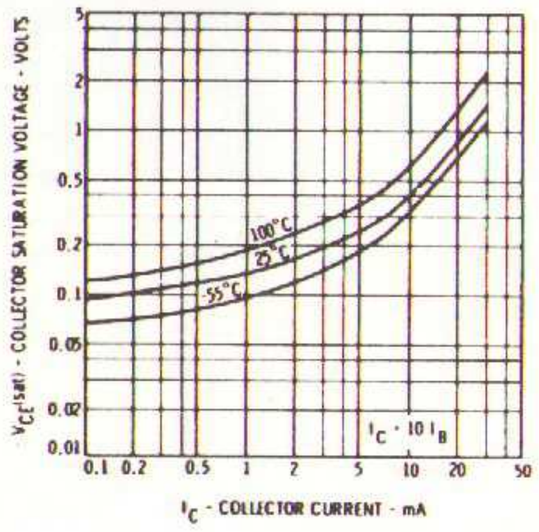
COLLECTOR-BASE DIODE REVERSE CURRENT VERSUS TEMPERATURE



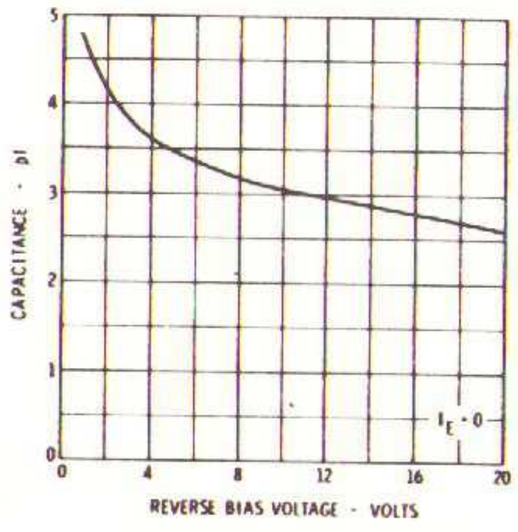
BASE-EMITTER ON VOLTAGE VERSUS COLLECTOR CURRENT



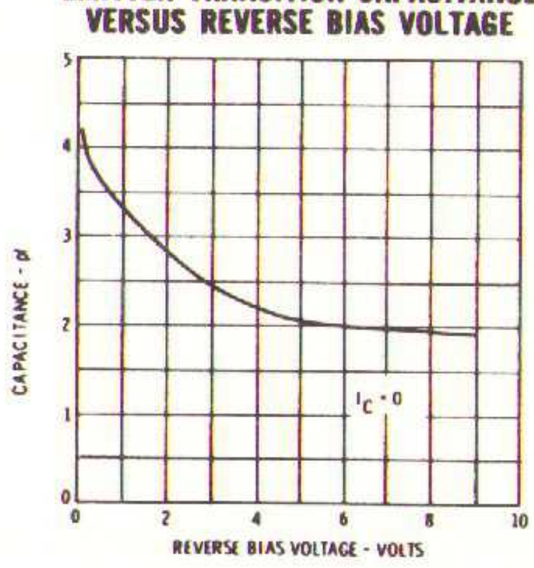
COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



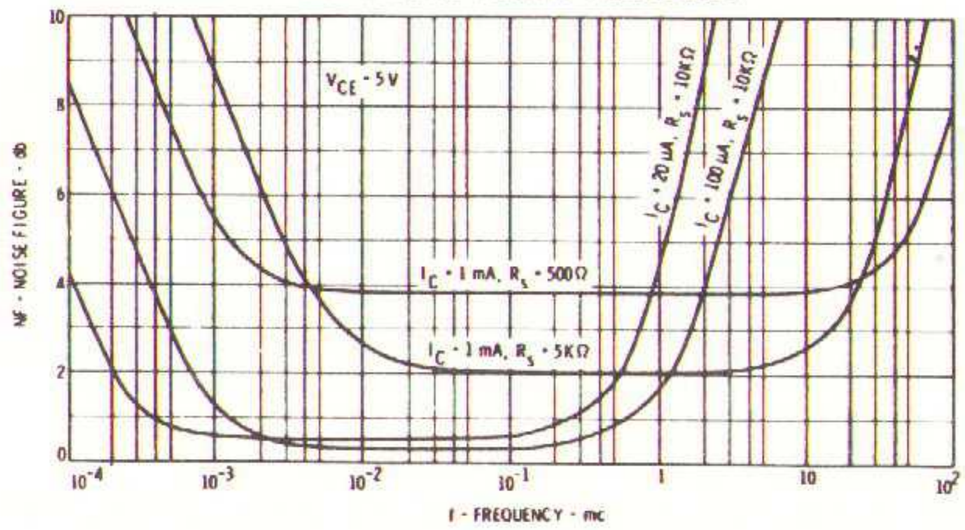
OUTPUT CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



EMITTER TRANSITION CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



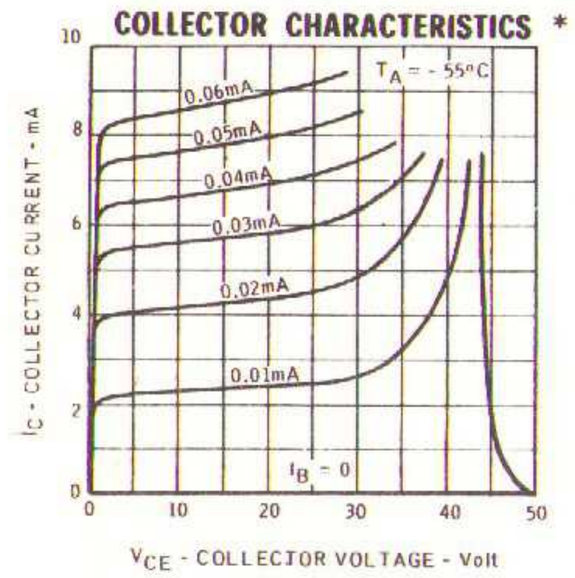
NOISE FIGURE VERSUS FREQUENCY



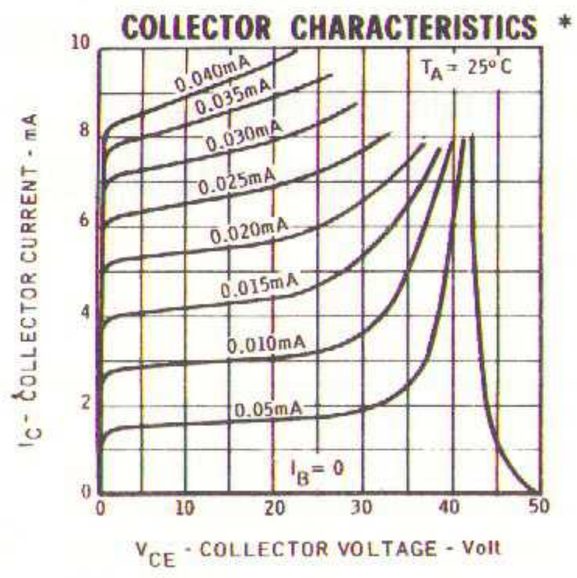
2C 415 SGS-FAIRCHILD PLANAR TRANSISTORS

TYPICAL ELECTRICAL CHARACTERISTICS

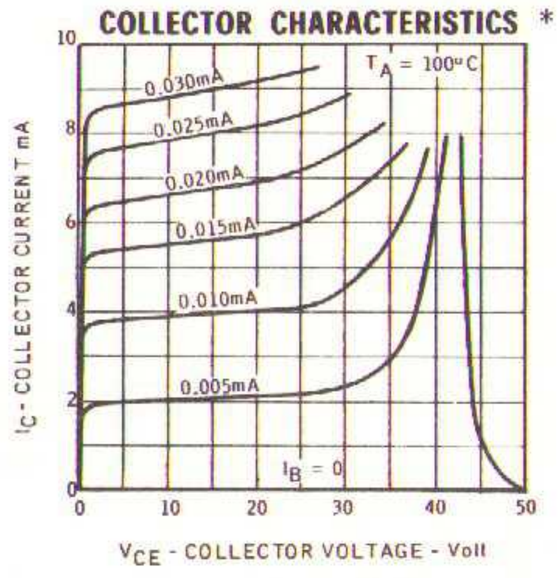
COLLECTOR CHARACTERISTICS *



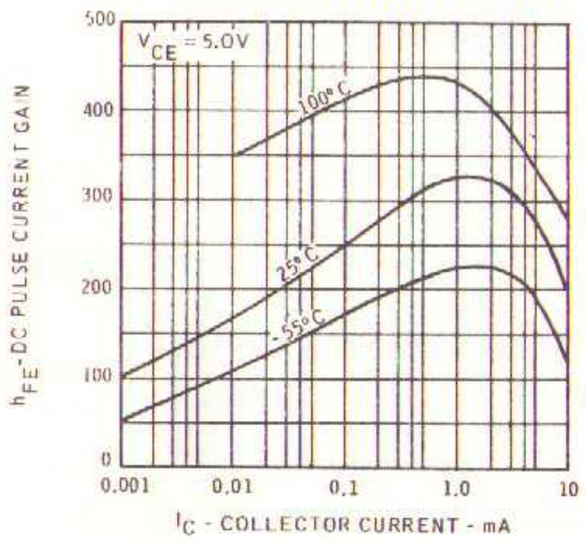
COLLECTOR CHARACTERISTICS *



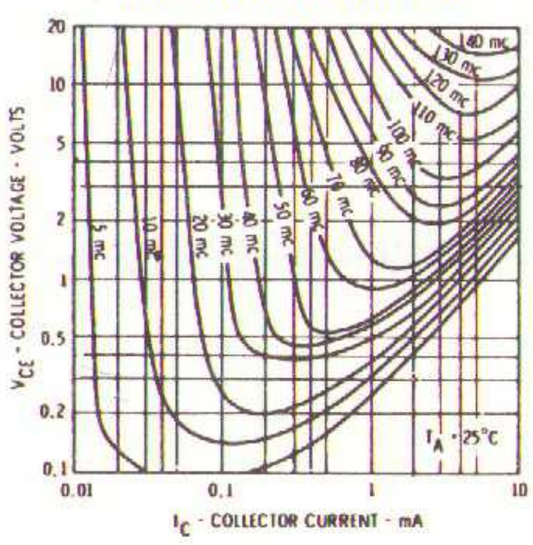
COLLECTOR CHARACTERISTICS *



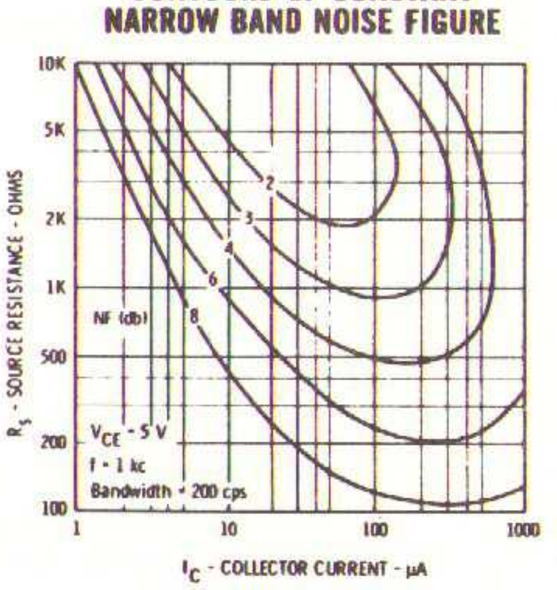
PULSED DC CURRENT GAIN VERSUS COLLECTOR CURRENT



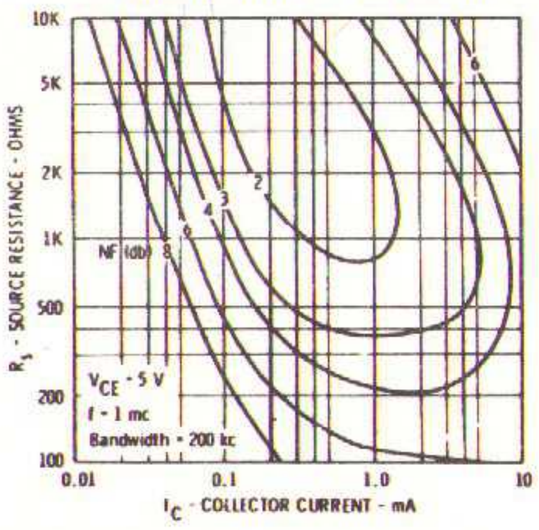
CONTOURS OF CONSTANT BANDWIDTH PRODUCT (f_T)



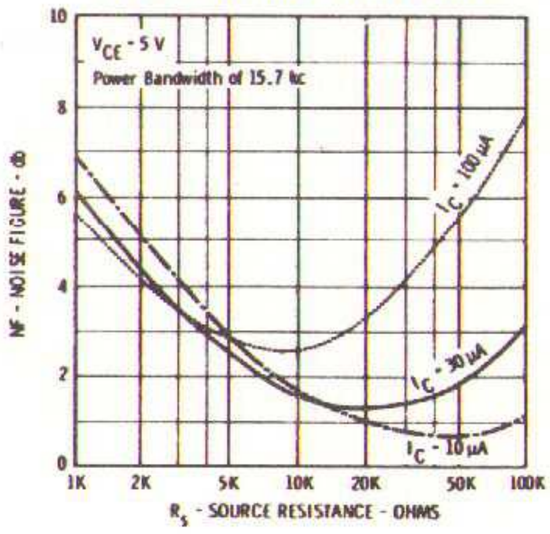
CONTOURS OF CONSTANT NARROW BAND NOISE FIGURE



CONTOURS OF CONSTANT NARROW BAND NOISE FIGURE



WIDE BAND NOISE FIGURE VERSUS SOURCE RESISTANCE

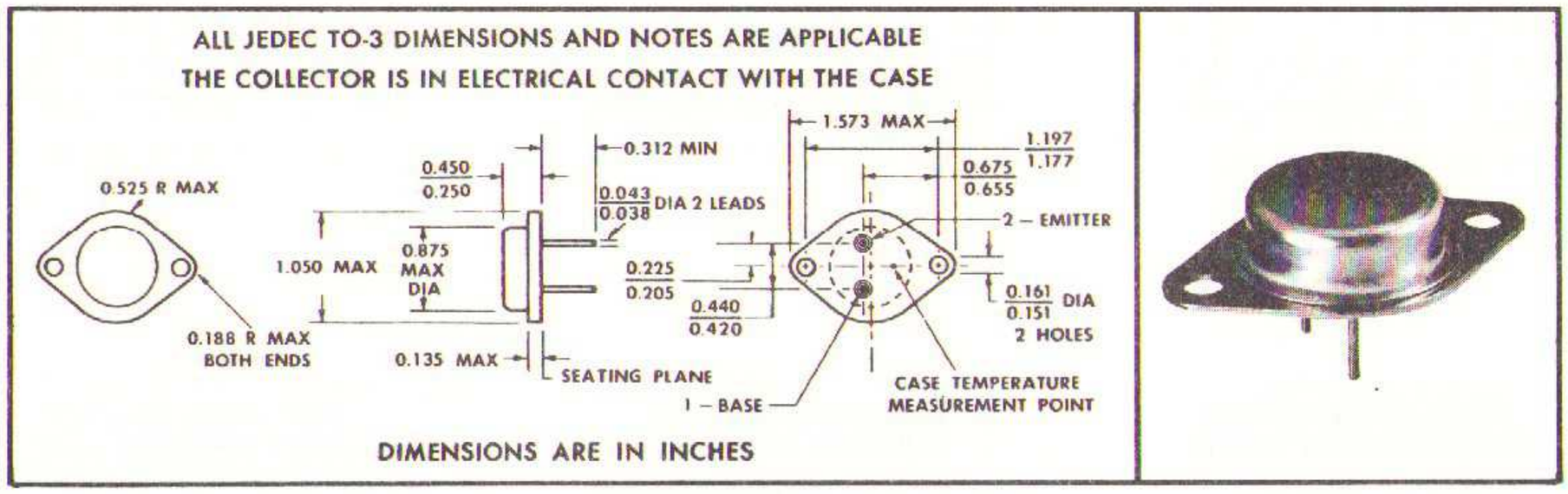


TYPES 2N4904, 2N4905, 2N4906
P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N4913, 2N4914, 2N4915

- **87.5 W at 25°C Case Temperature**
- **5 A Rated Collector Current**
- **Min f_T of 4 MHz at 10 V, 500 mA**

***mechanical data**



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N4904	2N4905	2N4906
*Collector-Base Voltage	-40 V	-60 V	-80 V
*Collector-Emitter Voltage (See Note 1)	-40 V	-80 V	-80 V
*Emitter-Base Voltage	← -5 V →		
*Continuous Collector Current	← -5 A →		
Peak Collector Current (See Note 2)	← -15 A →		
*Continuous Base Current	← -1 A →		
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 2 →		
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 87.5 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 4 W →		
*Operating Collector Junction Temperature Range	← -65°C to 200°C →		
*Storage Temperature Range	← -65°C to 200°C →		
*Lead Temperature 1/16 Inch from Case for 10 Seconds	← 235°C →		

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 0.5 W/deg.
4. Derate linearly to 200°C free-air temperature at the rate of 22.9 mW/deg.

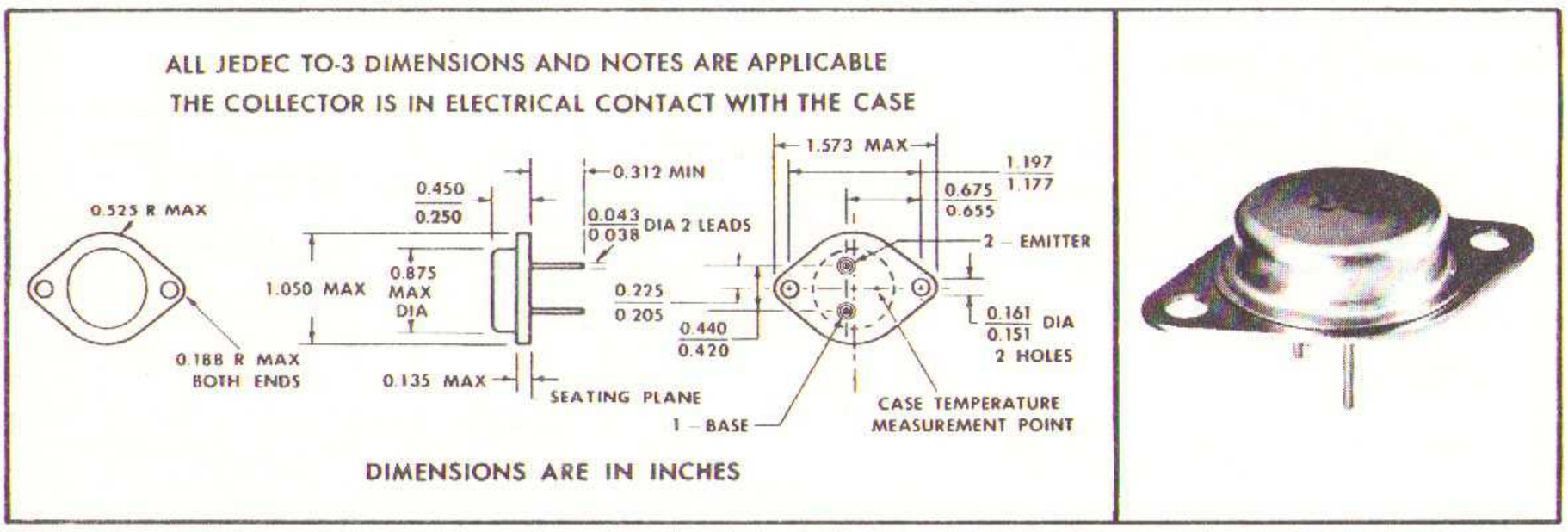
*Indicates JEDEC registered data

TYPES 2N4913, 2N4914, 2N4915
N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N4904 THRU 2N4906

- **87.5 W at 25°C Case Temperature**
- **5 A Rated Collector Current**
- **Min f_T of 4 MHz at 10 V, 1 A**

***mechanical data**



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N4913	2N4914	2N4915
*Collector-Base Voltage	40 V	60 V	80 V
*Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V
*Emitter-Base Voltage	←	5 V	→
*Continuous Collector Current	←	5 A	→
Peak Collector Current (See Note 2)	←	15 A	→
*Continuous Base Current	←	1 A	→
Safe Operating Region at (or below) 25°C Case Temperature	←	See Figure 6	→
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	←	87.5 W	→
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	←	4 W	→
*Operating Collector Junction Temperature Range	←	−65°C to 200°C	→
*Storage Temperature Range	←	−65°C to 200°C	→
*Lead Temperature 1/16 Inch from Case for 10 Seconds	←	235°C	→

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_p = 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 0.5 W/deg.
4. Derate linearly to 200°C free-air temperature at the rate of 22.9 mW/deg.

*Indicates JEDEC registered data

TYPES 2N4913, 2N4914, 2N4915
N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

***electrical characteristics at 25°C case temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS			2N4913 MIN	2N4913 MAX	2N4914 MIN	2N4914 MAX	2N4915 MIN	2N4915 MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 200 mA,	I_B = 0,	See Note 5	40		60		80		V
I_{CEO}	Collector Cutoff Current	V_{CE} = 40 V,	I_B = 0			1					mA
		V_{CE} = 60 V,	I_B = 0					1			
		V_{CE} = 80 V,	I_B = 0							1	
I_{CEV}	Collector Cutoff Current	V_{CE} = 40 V,	V_{BE} = −1.5 V			0.1					mA
		V_{CE} = 60 V,	V_{BE} = −1.5 V					0.1			
		V_{CE} = 80 V,	V_{BE} = −1.5 V							0.1	
		V_{CE} = 40 V,	V_{BE} = −1.5 V,	T_C = 150°C		2					
		V_{CE} = 60 V,	V_{BE} = −1.5 V,	T_C = 150°C				2			
		V_{CE} = 80 V,	V_{BE} = −1.5 V,	T_C = 150°C						2	
I_{EBO}	Emitter Cutoff Current	V_{EB} = 5 V,	I_C = 0			1		1		1	mA
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 2 V,	I_C = 2.5 A,	See Notes 5 and 6	25	100	25	100	25	100	
		V_{CE} = 2 V,	I_C = 5 A,	See Notes 5 and 6	7		7		7		
V_{BE}	Base-Emitter Voltage	V_{CE} = 2 V,	I_C = 2.5 A,	See Notes 5 and 6		1.4		1.4		1.4	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 0.25 A,	I_C = 2.5 A,	See Notes 5 and 6		0.75		0.75		0.75	V
		I_B = 1 A,	I_C = 5 A,	See Notes 5 and 6		1.5		1.5		1.5	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	V_{CE} = 10 V,	I_C = 0.5 A,	f = 1 kHz	20		20		20		
$\lvert h_{fe} \rvert$	Small-Signal Common-Emitter Forward Current Transfer Ratio	V_{CE} = 10 V,	I_C = 1 A,	f = 1 MHz	4		4		4		

NOTES: 5. These parameters must be measured using pulse techniques. t_p = 300 μs, duty cycle ≤ 2%.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER		MAX	UNIT
$\theta_{J\text{-}C}$	Junction-to-Case Thermal Resistance	2	deg/W
$\theta_{J\text{-}A}$	Junction-to-Free-Air Thermal Resistance	43.7	

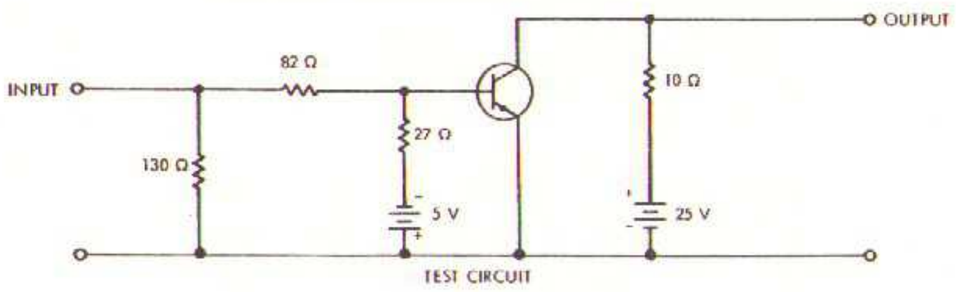
*Indicates JEDEC registered data

switching characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS†			TYP	UNIT
t_{on}	Turn-On Time	I_C = 2.5 A,	$I_{B(1)}$ = 250 mA,	$I_{B(2)}$ = −250 mA,	0.6	μs
t_{off}	Turn-Off Time	$V_{BE(off)}$ = −4.1 V,	R_L = 10 Ω,	See Figure 1	1.2	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



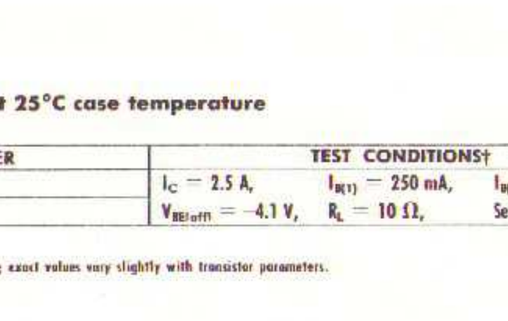


FIGURE 1

NOTES: a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, Z_{out} = 50 Ω, t_p = 10 μs, duty cycle < 2%.

b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ MΩ, $C_{in} \leq 11.5$ pF.

c. Resistors must be noninductive types.

d. The d-c power supplies may require additional bypassing in order to minimize ringing.

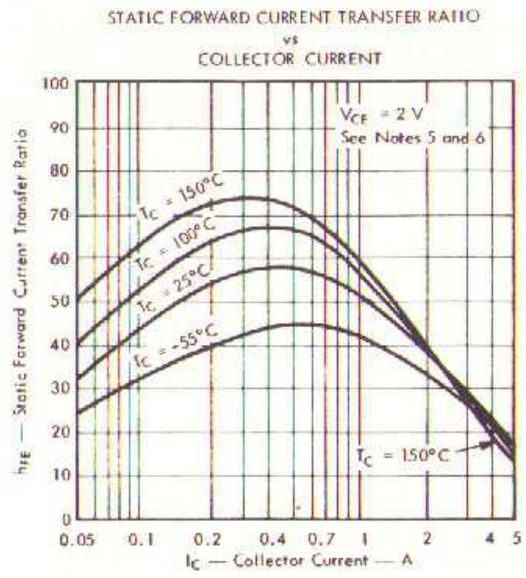


FIGURE 2

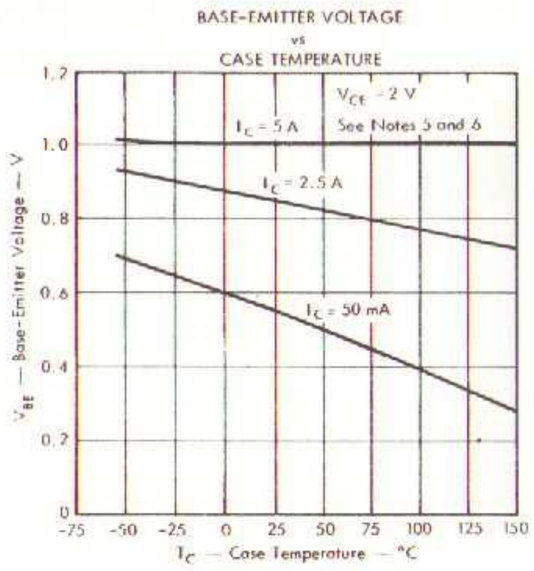


FIGURE 3

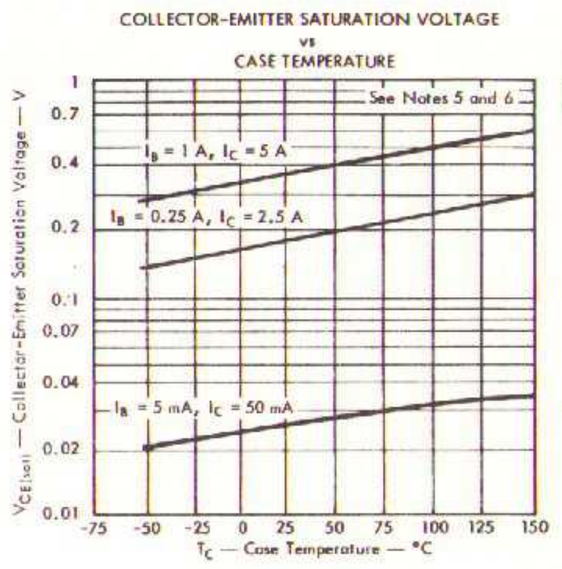


FIGURE 4

NOTES: 5. These parameters must be measured using pulse techniques. t_p = 300 μs, duty cycle ≤ 2%.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

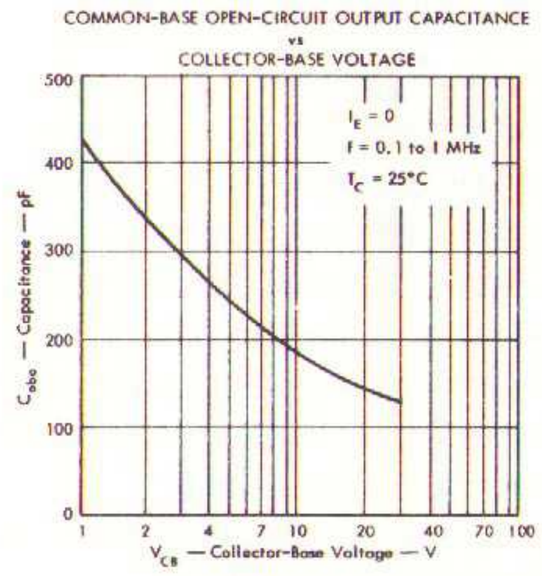


FIGURE 5

MAXIMUM SAFE OPERATING REGION

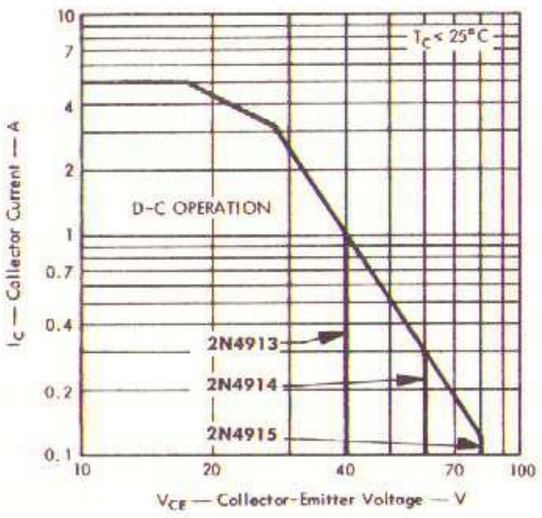


FIGURE 6

TYPES 2N4913, 2N4914, 2N4915
N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

THERMAL INFORMATION

DISSIPATION DERATING CURVE

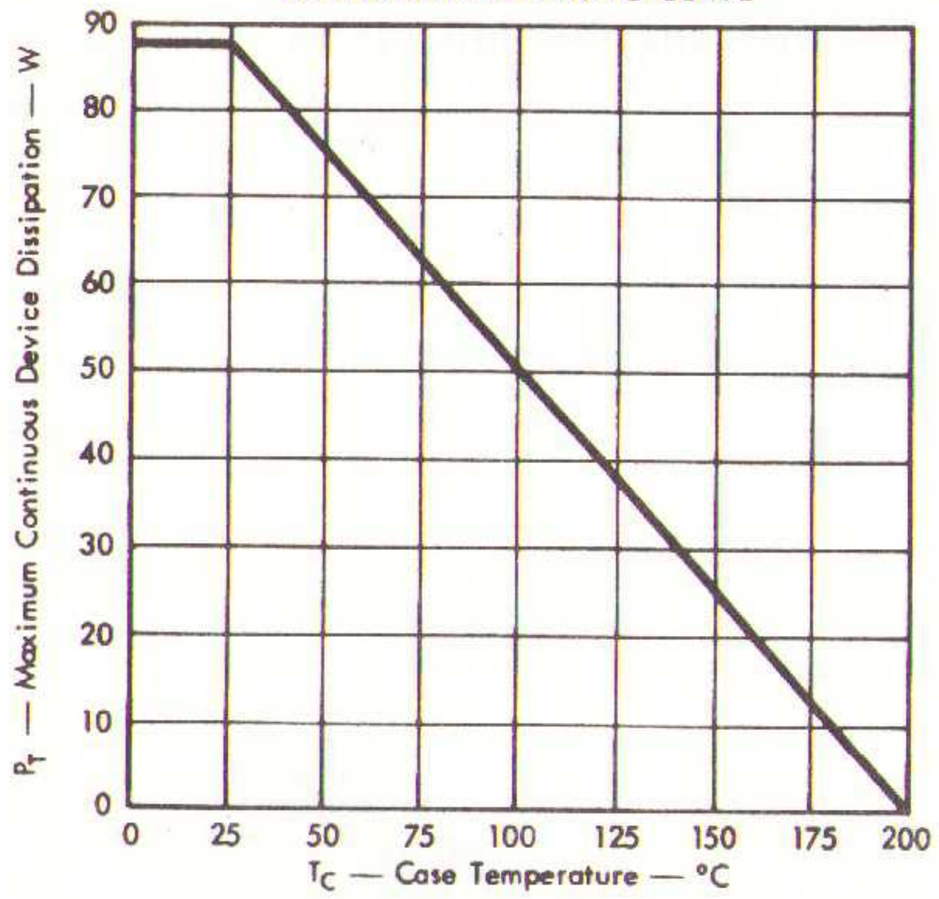


FIGURE 7

PEAK-POWER COEFFICIENT CURVE

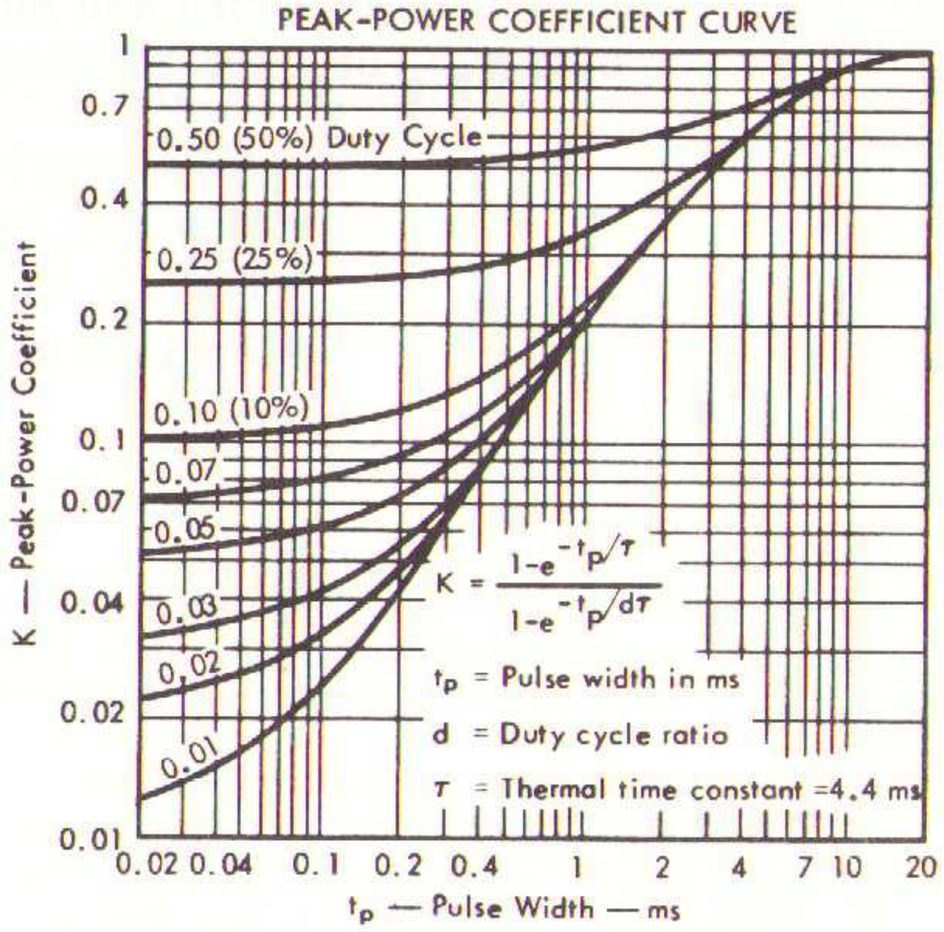


FIGURE 8

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
$\theta_{J\text{-}A}$	Junction-to-Free-Air Thermal Resistance	43.7	deg/W
$\theta_{J\text{-}C}$	Junction-to-Case Thermal Resistance	2	deg/W
$\theta_{C\text{-}A}$	Case-to-Free-Air Thermal Resistance	41.7	deg/W
$\theta_{C\text{-}HS}$	Case-to-Heat-Sink Thermal Resistance		deg/W
$\theta_{HS\text{-}A}$	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	$\leq$ 200	°C
$T_{J(max)}$	Peak Junction Temperature	$\leq$ 200	°C
K	Peak-Power Coefficient	See Figure 8	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty Cycle Ratio (t_p/t_x)		

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J\text{-}C} + \theta_{C\text{-}HS} + \theta_{HS\text{-}A}} \quad \text{for } 25\,^\circ\text{C} \leq T_C \leq 200\,^\circ\text{C}, \text{ as in figure 7.}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J\text{-}A}} \quad \text{for } 25\,^\circ\text{C} \leq T_A \leq 200\,^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\,(\theta_{C\text{-}HS} + \theta_{HS\text{-}A}) + K\,\theta_{J\text{-}C}} \quad \text{for } 25\,^\circ\text{C} \leq T_C \leq 200\,^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\,\theta_{C\text{-}A} + K\,\theta_{J\text{-}C}} \quad \text{for } 25\,^\circ\text{C} \leq T_A \leq 200\,^\circ\text{C}$$

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$\theta_{C\text{-}HS} + \theta_{HS\text{-}A} = 2.25$ deg/W (From information supplied with heat sink.)

$T_{J(av)}$ (design limit) = 200°C

$T_A = 50\,^\circ\text{C}$

d = 10% (0.1)

$t_p = 0.1$ ms

Solution:

From figure 8, Peak-Power Coefficient

K = 0.11 and by use of equation No. 3

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\,(\theta_{C\text{-}HS} + \theta_{HS\text{-}A}) + K\,\theta_{J\text{-}C}}$$

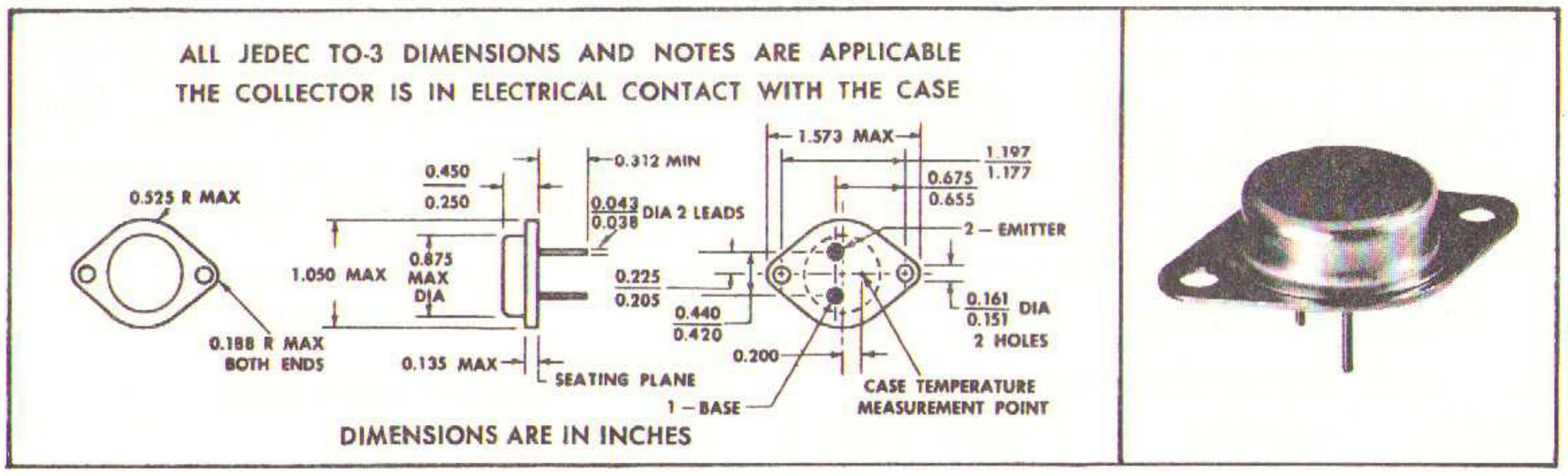
$$P_{T(max)} = \frac{200 - 50}{0.1(2.25) + 0.11(2)} = 337 \text{ W}$$

TYPES 2N3789, 2N3790, 2N3791, 2N3792
P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N3713 THRU 2N3716

- **150 Watts at 25°C Case Temperature**
- **10 A Rated Collector Current**
- **Min f_T of 4 MHz at 10 V, 500 mA**
- **Min f_{hfe} of 30 kHz at 10 V, 500 mA**

***mechanical data**



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3789 2N3791	2N3790 2N3792
*Collector-Base Voltage	-60 V	-80 V
*Collector-Emitter Voltage (See Note 1)	-60 V	-80 V
*Emitter-Base Voltage	← -7 V →	
*Continuous Collector Current	← -10 A →	
Peak Collector Current (See Note 2)	← -15 A →	
*Continuous Base Current	← -4 A →	
*Safe Operating Region at (or below) 25°C Case Temperature	See Figures 6 and 7	
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 150 W →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 4 W →	
*Operating Collector Junction Temperature Range	-65°C to 200°C	
*Storage Temperature Range	-65°C to 200°C	
Lead Temperature 1/16 Inch from Case for 10 Seconds	← 235°C →	

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_p = 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 0.855 W/deg.
4. Derate linearly to 200°C free-air temperature at the rate of 22.9 mW/deg.

*Indicates JEDEC registered data

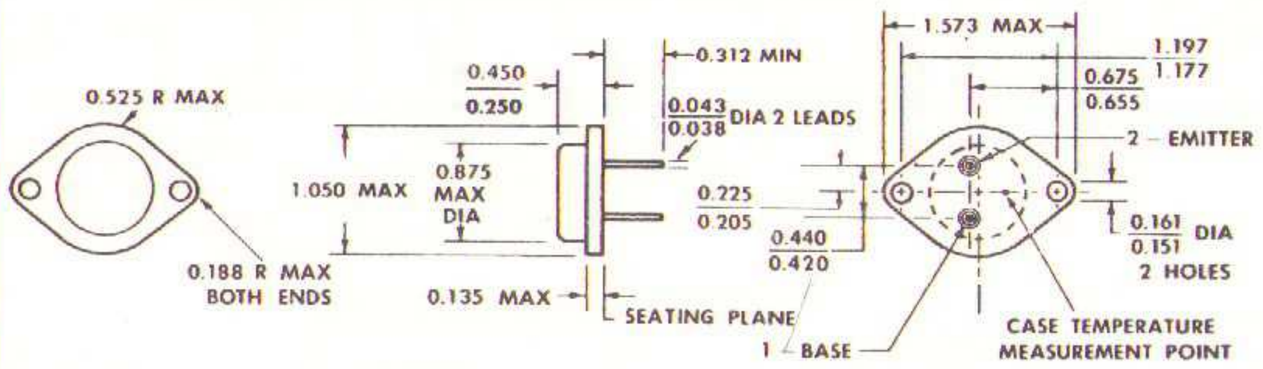
TYPES 2N3713, 2N3714, 2N3715, 2N3716
N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND SWITCHING APPLICATIONS

- **150 W at 25°C Case Temperature**
- **10 A Rated Collector Current**
- **Min f_{hfe} of 30 kHz**
- **Min f_T of 4 MHz**

***mechanical data**

ALL JEDEC TO-3 DIMENSIONS AND NOTES ARE APPLICABLE
THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE



DIMENSIONS ARE IN INCHES

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3713	2N3714	2N3715	2N3716
*Collector-Base Voltage	80 V	100 V	80 V	100 V
*Collector-Emitter Voltage (See Note 1)	60 V	80 V	60 V	80 V
*Emitter-Base Voltage	7 V			
*Continuous Collector Current	10 A			
Peak Collector Current (See Note 2)	15 A			
*Continuous Base Current	4 A			
*Safe Operating Region at (or below) 25°C Case Temperature	See Figures 8 and 9			
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	150 W			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	4 W			
*Operating Collector Junction Temperature Range	−65°C to 200°C			
*Storage Temperature Range	−65°C to 200°C			
Lead Temperature 1/16 Inch from Case for 10 Seconds	235°C			

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_p = 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 0.855 W/deg.
4. Derate linearly to 200°C free-air temperature at the rate of 22.9 mW/deg.

*Indicates JEDEC registered data

TYPES 2N3713, 2N3714, 2N3715, 2N3716
N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	2N3713 MIN	2N3713 MAX	2N3714 MIN	2N3714 MAX	2N3715 MIN	2N3715 MAX	2N3716 MIN	2N3716 MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 200 mA, I_B = 0, See Note 5	60		80		60		80		V
I_{CEO}	Collector Cutoff Current	V_{CE} = 30 V, I_B = 0		0.7				0.7			mA
		V_{CE} = 40 V, I_B = 0				0.7				0.7	
I_{CEV}	Collector Cutoff Current	V_{CE} = 80 V, V_{BE} = −1.5 V		1				1			mA
		V_{CE} = 100 V, V_{BE} = −1.5 V				1				1	
		V_{CE} = 60 V, V_{BE} = −1.5 V, T_C = 150°C		10				10			mA
		V_{CE} = 80 V, V_{BE} = −1.5 V, T_C = 150°C				10				10	
I_{EBO}	Emitter Cutoff Current	V_{EB} = 7 V, I_C = 0		1		1		1		1	mA
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 2 V, I_C = 1 A, See Notes 5 and 6	25	75	25	75	50	150	50	150	
		V_{CE} = 2 V, I_C = 3 A, See Notes 5 and 6	15		15		30		30		
		V_{CE} = 4 V, I_C = 10 A, See Notes 5 and 6	5		5		5		5		
V_{BE}	Base-Emitter Voltage	V_{CE} = 2 V, I_C = 5 A, See Notes 5 and 6		2		2		1.8		1.8	V
		V_{CE} = 4 V, I_C = 10 A, See Notes 5 and 6		4		4		4		4	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 0.5 A, I_C = 5 A, See Notes 5 and 6		1		1		0.8		0.8	V
		I_B = 2 A, I_C = 10 A, See Notes 5 and 6		4		4		4		4	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	V_{CE} = 10 V, I_C = 0.5 A, f = 1 kHz	25	250	25	250	25	250	25	250	
$\lvert h_{fe} \rvert$	Small-Signal Common-Emitter Forward Current Transfer Ratio	V_{CE} = 10 V, I_C = 0.5 A, f = 1 MHz	4		4		4		4		
f_{hfe}	Small-Signal Common-Emitter Forward Current Transfer Ratio Cutoff Frequency	V_{CE} = 10 V, I_C = 0.5 A	30		30		30		30		kHz
C_{obo}	Common-Base Open-Circuit Output Capacitance	V_{CB} = 10 V, I_E = 0, f = 100 kHz		250		250		250		250	pF

NOTES: 5. These parameters must be measured using pulse techniques. t_p = 300 μs, duty cycle ≤ 2%.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER		MAX	UNIT
$\theta_{J\text{-}C}$	Junction-to-Case Thermal Resistance	1.17	deg/W
$\theta_{J\text{-}A}$	Junction-to-Free-Air Thermal Resistance	43.7	

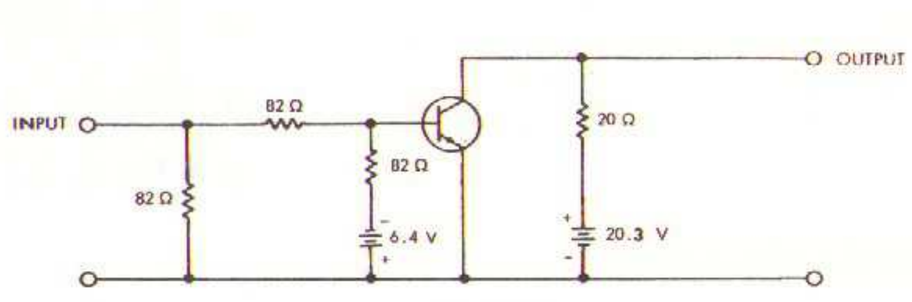
*Indicates JEDEC registered data

switching characteristics at 25°C case temperature

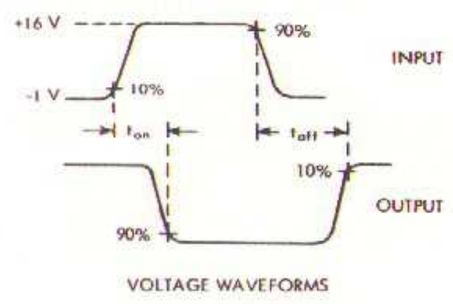
PARAMETER		TEST CONDITIONS†	TYP	UNIT
t_{on}	Turn-On Time	I_C = 1 A, $I_{B(1)}$ = 100 mA, $I_{B(2)}$ = −100 mA, $V_{BE(off)}$ = −3.7 V, R_L = 20 Ω, See Figure 1	450	ns
t_{off}	Turn-Off Time		350	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

NOTES: a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, Z_{out} = 50 Ω, t_p = 10 μs, duty cycle ≤ 2%.
b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ MΩ, $C_{in} \leq 11.5$ pF.
c. Resistors must be noninductive types.
d. The d-c power supplies may require additional bypassing in order to minimize ringing.

2N3713, 2N3714
STATIC FORWARD CURRENT TRANSFER RATIO vs COLLECTOR CURRENT

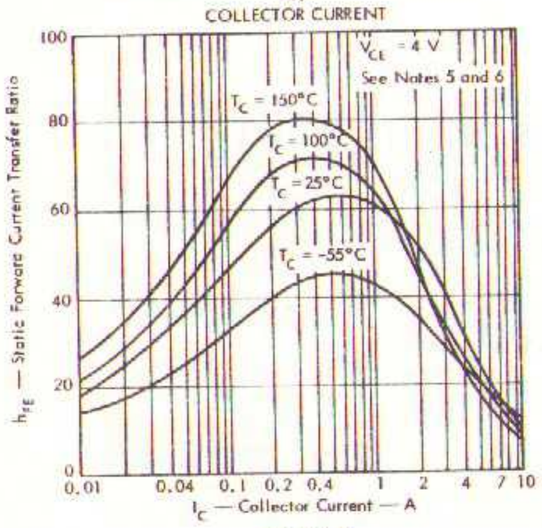


FIGURE 2

2N3715, 2N3716
STATIC FORWARD CURRENT TRANSFER RATIO vs COLLECTOR CURRENT

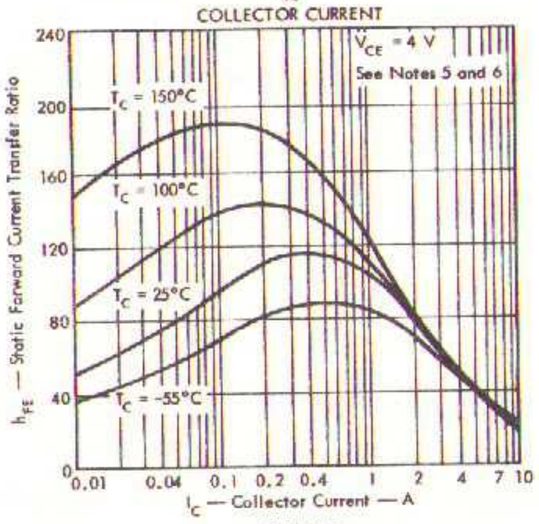


FIGURE 3

NORMALIZED COLLECTOR-EMITTER BREAKDOWN VOLTAGE vs BASE-EMITTER RESISTANCE

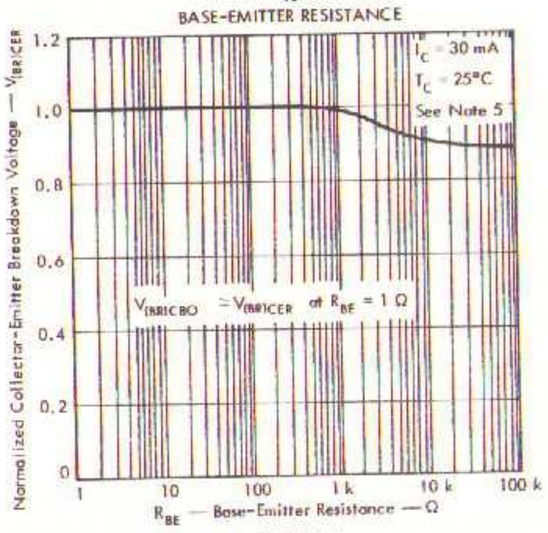


FIGURE 6

COMMON-BASE OPEN-CIRCUIT OUTPUT CAPACITANCE vs COLLECTOR-BASE VOLTAGE

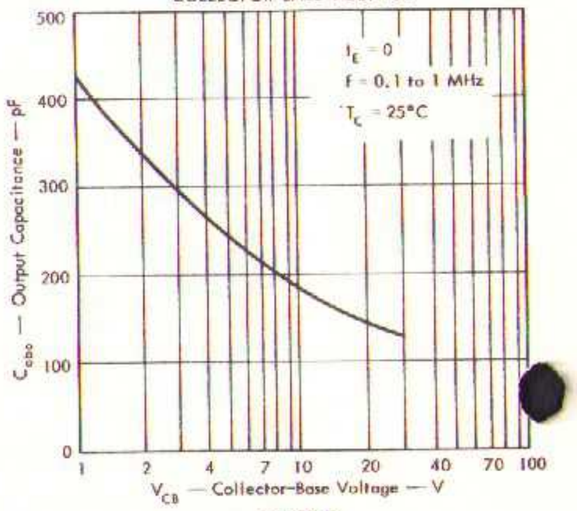


FIGURE 7

MAXIMUM SAFE OPERATING REGIONS

2N3713, 2N3715

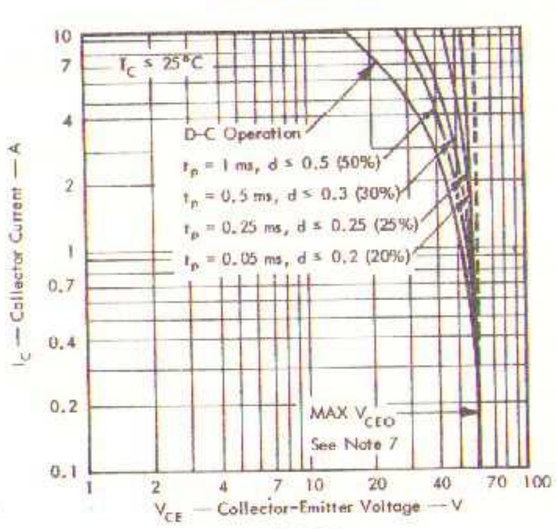


FIGURE 8

2N3714, 2N3716

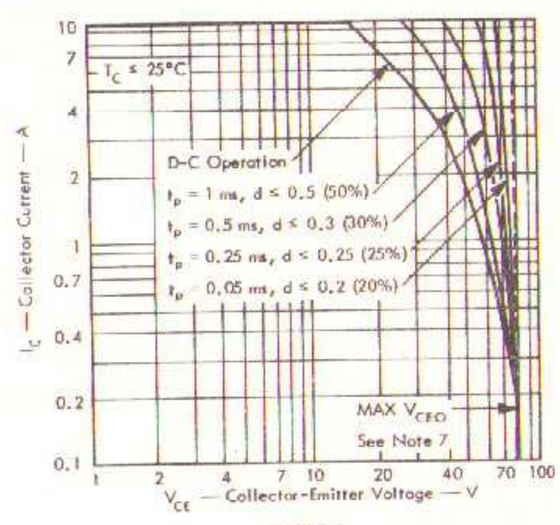


FIGURE 9

BASE-EMITTER VOLTAGE vs CASE TEMPERATURE

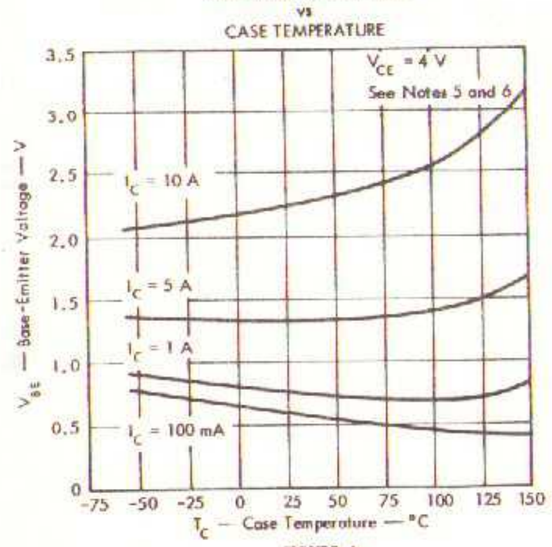


FIGURE 4

COLLECTOR-EMITTER SATURATION VOLTAGE vs CASE TEMPERATURE

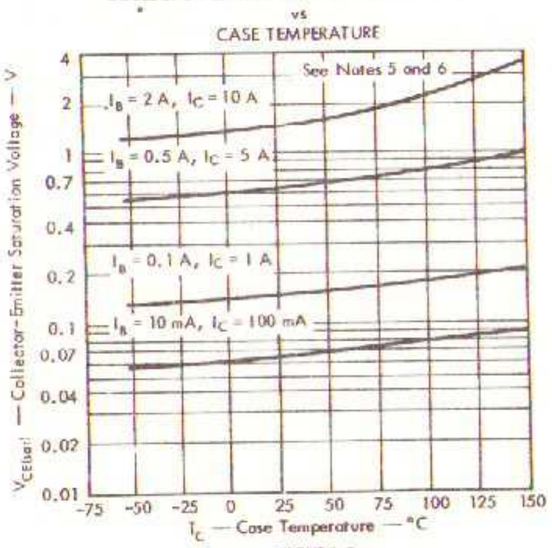


FIGURE 5

NOTES: 5. These parameters must be measured using pulse techniques. t_p = 300 μs, duty cycle ≤ 2%.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

NOTES: 5. This parameter must be measured using pulse techniques. t_p = 300 μs, duty cycle ≤ 2%.
7. Operation above maximum V_{CEO} is permissible if the base is reverse-voltage biased with respect to the emitter and the collector-base-voltage rating is not exceeded.

TYPES 2N3713, 2N3714, 2N3715, 2N3716
N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

THERMAL INFORMATION

DISSIPATION DERATING CURVE

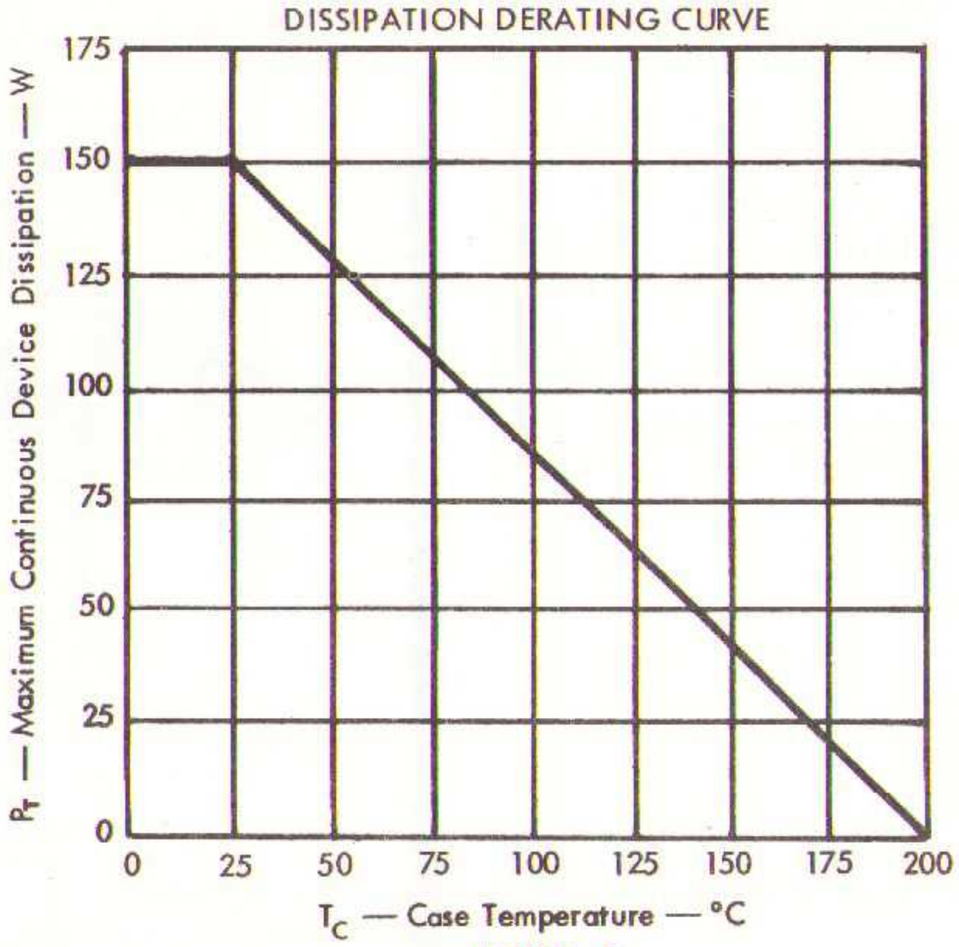


FIGURE 10

PEAK-POWER COEFFICIENT CURVE

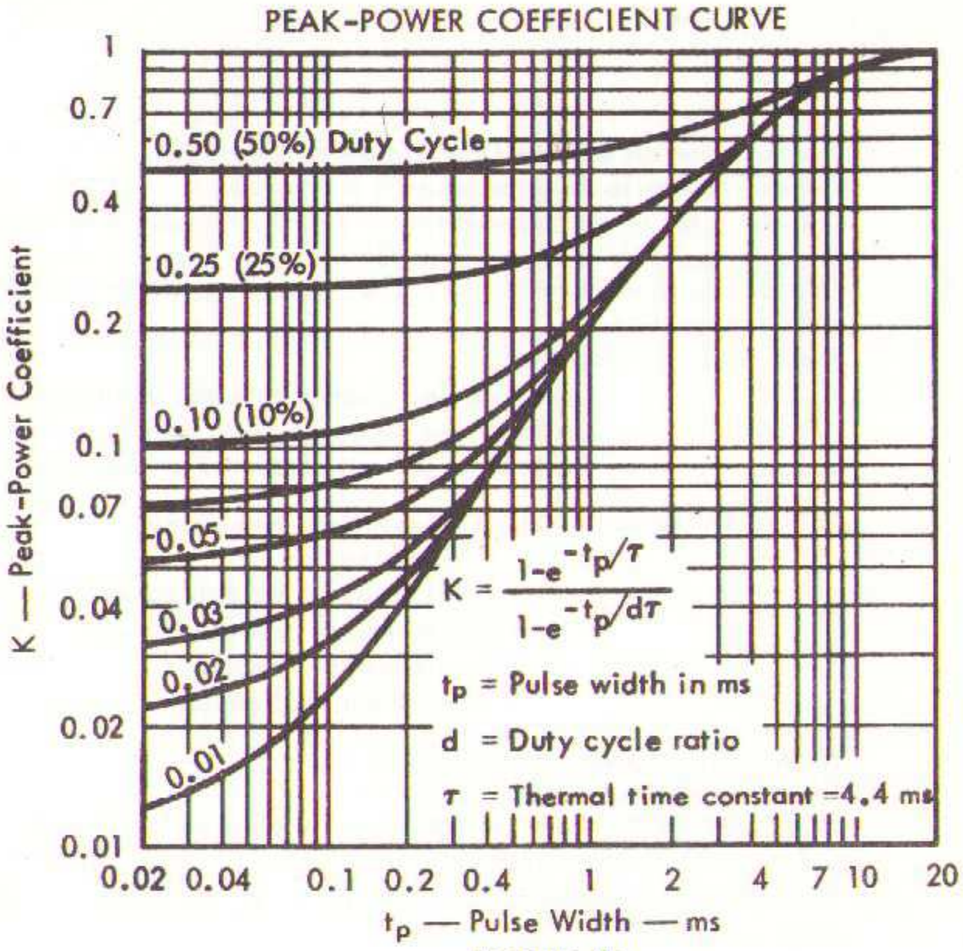


FIGURE 11

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
$\theta_{J\text{-}A}$	Junction-to-Free-Air Thermal Resistance	43.7	deg/W
$\theta_{J\text{-}C}$	Junction-to-Case Thermal Resistance	1.17	deg/W
$\theta_{C\text{-}A}$	Case-to-Free-Air Thermal Resistance	42.5	deg/W
$\theta_{C\text{-}HS}$	Case-to-Heat-Sink Thermal Resistance		deg/W
$\theta_{HS\text{-}A}$	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 11	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty Cycle Ratio (t_p/t_x)		

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J\text{-}C} + \theta_{C\text{-}HS} + \theta_{HS\text{-}A}} \quad \text{for } 25\,^\circ\text{C} \leq T_C \leq 200\,^\circ\text{C}, \text{ as in figure 10.}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J\text{-}A}} \quad \text{for } 25\,^\circ\text{C} \leq T_A \leq 200\,^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\,(\theta_{C\text{-}HS} + \theta_{HS\text{-}A}) + K\,\theta_{J\text{-}C}} \quad \text{for } 25\,^\circ\text{C} \leq T_C \leq 200\,^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\,\theta_{C\text{-}A} + K\theta_{J\text{-}C}} \quad \text{for } 25\,^\circ\text{C} \leq T_A \leq 200\,^\circ\text{C}$$

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$\theta_{C\text{-}HS} + \theta_{HS\text{-}A} = 2.25$ deg/W (From information supplied with heat sink.)

$T_{J(av)}$ (design limit) $= 200\,^\circ\text{C}$

$T_A = 50\,^\circ\text{C}$

d = 10% (0.1)

$t_p = 0.1$ ms

Solution:

From figure 11, Peak-Power Coefficient

K = 0.11 and by use of equation No. 3

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\,(\theta_{C\text{-}HS} + \theta_{HS\text{-}A}) + K\,\theta_{J\text{-}C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(2.25) + 0.11(1.17)} = 424 \text{ W}$$

SILICIUM

SILICON

TRANSISTORS NPN MESA DE PUISSANCE 175 W

175 W NPN MESA POWER TRANSISTORS

NOTICE PRELIMINAIRE
PRELIMINARY SPECIFICATION

108 T 2
109 T 2

- **Forte tenue en tension (supérieure à 160 volts).**
- **Grande linéarité de gain jusqu'à 6 ampères.**
- **Grande vitesse de commutation : t_{on} 0,2 μs moyen à 15 ampères.**
- **Aire de sécurité parfaitement définie pour tous les domaines d'application.**
- **Impédance thermique faible 0,6° C/W moyen et parfaitement stable dans les épreuves de cycles thermiques.**
- **Haut degré de fiabilité.**
- **Soudure des connexions par ultrasons.**
- **Adaptation du coefficient de dilatation entre le cristal de silicium et l'embase par utilisation d'un intermédiaire en molybdène.**

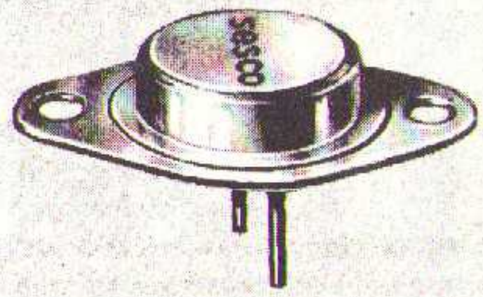
APPLICATIONS :

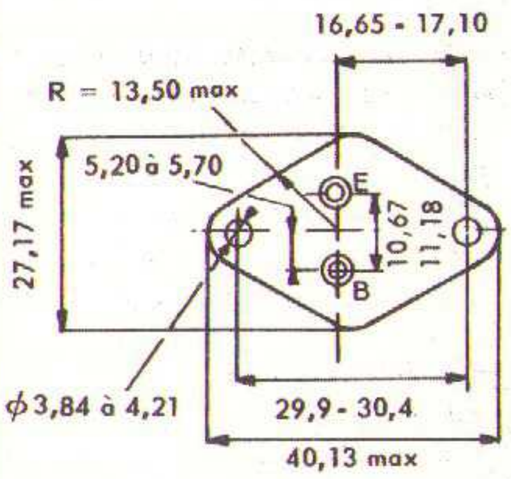
- **Alimentation stabilisée**
- **Convertisseur**
- **Amplificateur de puissance**
- **Commutation de puissance.**
- **Amplificateur de son**
- **Générateur d'ultrason.**

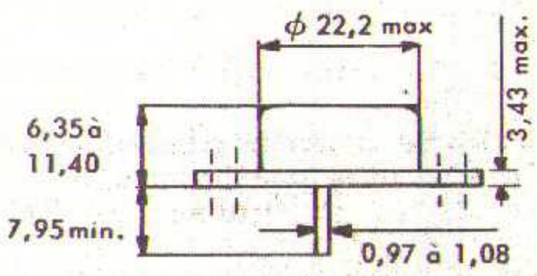
- *High voltage level, minimum 160 volts.*
- *Good linear gain to up 6 amperes.*
- *High speed switching typical t_{on} 0,2 μS at 15 amperes.*
- *Safe operating area perfectly defined for all applications.*
- *Low thermal impedance, typical 0,6° C/W, perfectly stable under thermal stress.*
- *High reliability.*
- *Ultrasonic connection welding.*
- *Matched expansion coefficient between the silicon cristal and the stud by use of a molybden preform.*

APPLICATIONS :

- *Regulated D.C. power supply.*
- *Converter.*
- *Power amplifier.*
- *Power switch*
- *Sound amplifier.*
- *Ultrasonic generator.*







Dimensions en mm

LIMITES ABSOLUES D'UTILISATION A 25° C BOITIER (sauf indications contraires) ABSOLUTE MAXIMUM RATINGS AT 25° C CASE (unless otherwise specified)	SYMBOLES SYMBOLS	108 T2	109 T2	UNITES UNITS
Puissance admissible au collecteur *Collector power dissipation* - **à 25° C (boîtier)** *at 25° C (case)*	P_C	175	175	W
Résistance thermique jonction-boîtier *Thermal resistance junction-case*	R_{th}	1	1	°C/W
Tension collecteur-émetteur (base ouverte) *Collector to emitter voltage (open base)*	V_{CEO}	80	125	V
Tension collecteur-base (émetteur ouvert) *Collector to base voltage (open emitter)*	V_{CBO}	120	160	V
Tension émetteur-base (collecteur ouvert) *Emitter to base voltage (open collector)*	V_{EBO}	10	10	V
Courant collecteur *Collector current*	I_C	30	30	A
Courant base *Base current*	I_B	15	15	A
Température de la jonction en fonctionnement *Operating junction temperature*	t_J	- 40 + 200		°C
Température de stockage *Storage temperature*	t_{stg}	- 40 + 200		°C

Collecteur relié au boîtier
Collector is connected to case

Boîtier JEDEC TO 3
Package CEI C 14 B - B 18
F 24

Marquage : en clair
Marking : numerals indicate type numbers

Poids
Weight ≅ 25 g

Homologation Registration			Liste préférentielle Referenced by				
TYPES	MARINE	CCT	OTAN	GAMT*	CNET*	CEA	ORTF

*Socotel - Sotelec

Ces dispositifs sont soumis aux essais préconisés par la norme CCT 13 01 A
These devices are tested according to French standard specification CCT 13 01 A.

1.22380.46

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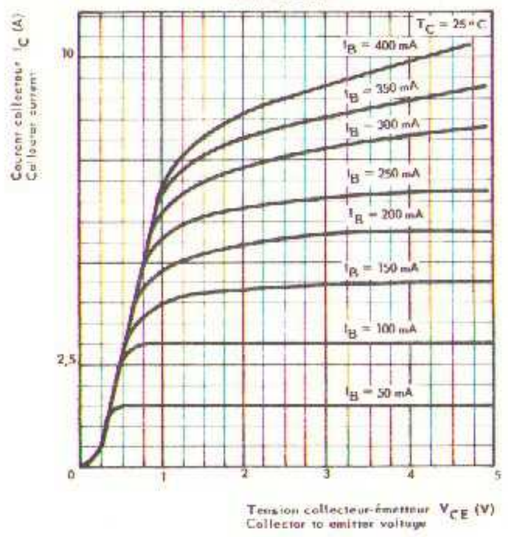
sesco

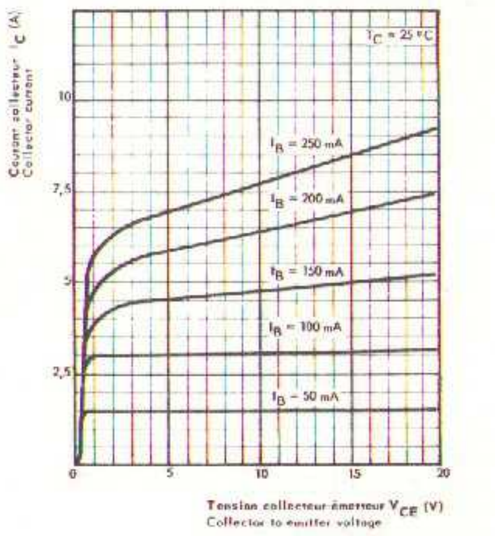
CARACTERISTIQUES ELECTRIQUES A 25°C BOITIER (sauf indications contraires) ELECTRICAL CHARACTERISTICS AT 25°C CASE (unless otherwise specified)	SYMBOLES SYMBOLS	108 T2 Min	108 T2 Moy Typ	108 T2 Max	109 T2 Min	109 T2 Moy Typ	109 T2 Max	UNITES UNITS
CARACTERISTIQUES STATIQUES *D.C. CHARACTERISTICS*								
Tension de claquage collecteur-émetteur (base ouverte) *Collector to emitter breakdown voltage (open base)* (I_C = 100 mA; I_B = 0)	$V_{(BR)CEO}$	80			125			V
Tension de claquage collecteur-base (émetteur ouvert) *Collector to base breakdown voltage (open emitter)* (I_C = 5 mA; I_E = 0)	$V_{(BR)CBO}$	120			160			V
Tension de claquage émetteur-base (collecteur ouvert) *Emitter to base breakdown voltage (open collector)* (I_E = 5 mA; I_C = 0)	$V_{(BR)EBO}$	10			10			V
Courant inverse collecteur-émetteur (R_{BE} = 10 Ω) *Collector to emitter cutoff current* (R_{BE} = 10 Ω) (V_{CE} = 80 V; I_B = 0; t_C = 100°C)	I_{CER}			10			10	mA
Courant inverse collecteur-base (émetteur ouvert) *Collector to base cutoff current (open emitter)* (V_{CB} = 120 V; I_E = 0)	I_{CBO}		0,5	1		0,5	1	mA
Courant inverse émetteur-base (collecteur ouvert) *Emitter to base cutoff current (open collector)* (V_{EB} = 10 V; I_C = 0)	I_{EBO}		0,25	5		0,25	5	mA
Gain en courant statique *D.C. current gain* (I_C = 10 A; V_{CE} = 4 V)	h_{21E}*	20		60	20		60	
(I_C = 10 A; V_{CE} = 4 V; t_C = -30° C)	h_{21E}*	10			10			
(I_C = 20 A; V_{CE} = 4 V)	h_{21E}*		15			15		
Tension de saturation collecteur-émetteur *Collector to emitter saturation voltage* (I_C = 10 A; I_B = 1 A)	$V_{CE(sat)}$		0,5	1,4		0,5	1,4	V
Tension de saturation base-émetteur *Base to emitter saturation voltage* (I_C = 10 A; I_B = 1 A)	$V_{BE(sat)}$		1,4	2		1,4	2	V
CARACTERISTIQUES DYNAMIQUES *DYNAMIC CHARACTERISTICS*								
Gain dynamique *Dynamic gain* (I_C = 1 A; V_{CE} = 15 V; f = 10 MHz)	h_{21e}	1	3		1	3		
CARACTERISTIQUES DE COMMUTATION *SWITCHING CHARACTERISTICS*								
Temps d'établissement (voir figure) *Turn on time (see circuit)* (I_C = 15 A; V_{CE} = 75 V; R_G = 5 Ω)	t_{on}		0,2			0,2		µs
Temps de coupure (voir figure) *Turn off time (see circuit)* (I_C = 15 A; V_{CE} = 75 V; R_G = 5 Ω)	t_{off}		0,7			0,7		µs

* Mesures en impulsions ⩽ 300 µs facteur de forme ⩽ 2 %
Pulse width ⩽ 300 µS, duty cycle ⩽ 2 %

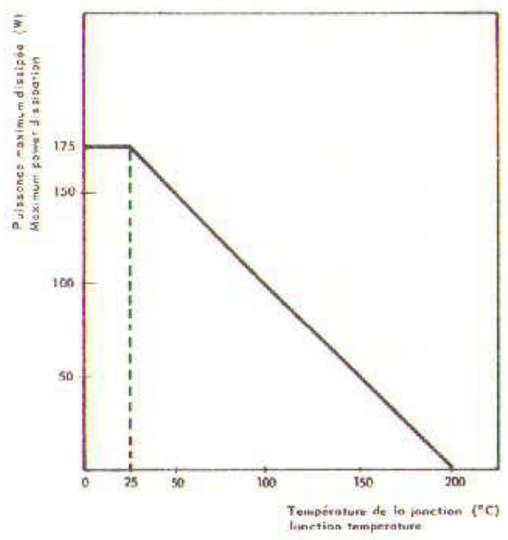
CARACTERISTIQUES STATIQUES EN EMETTEUR COMMUN
FAIBLE TENSION
STATIC CHARACTERISTICS (COMMON EMITTER)
LOW LEVEL



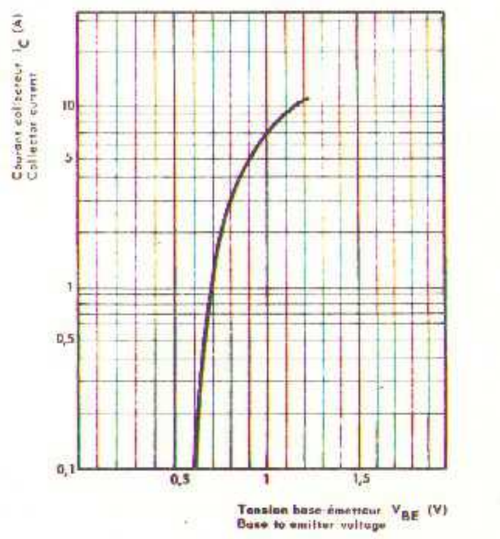
CARACTERISTIQUES STATIQUES EN EMETTEUR COMMUN
STATIC CHARACTERISTICS (COMMON EMITTER)



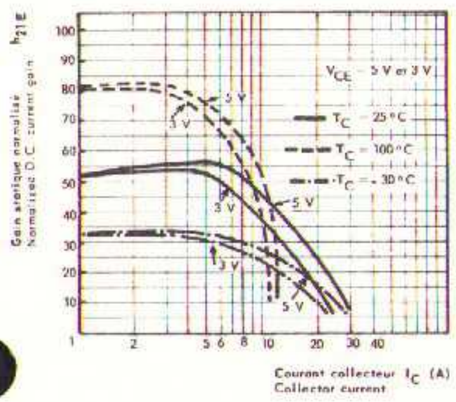
VARIATION DE LA PUISSANCE DISSIPEE EN FONCTION DE LA TEMPERATURE DU BOITIER
POWER DISSIPATION VERSUS CASE TEMPERATURE



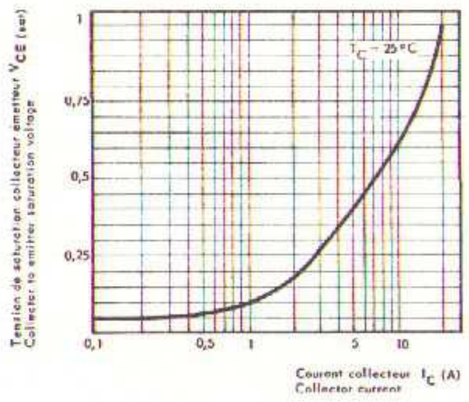
VARIATION DU COURANT COLLECTEUR EN FONCTION DE LA TENSION BASE-EMETTEUR
COLLECTOR CURRENT VERSUS
BASE TO EMITTER VOLTAGE



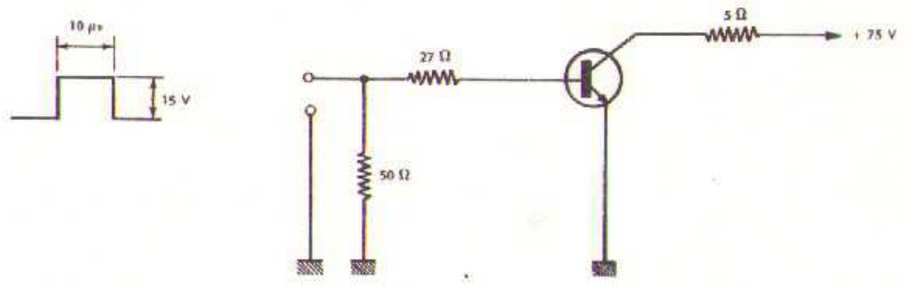
GAIN EN COURANT STATIQUE
EN FONCTION DU COURANT COLLECTEUR
D.C. CURRENT GAIN VERSUS COLLECTOR CURRENT



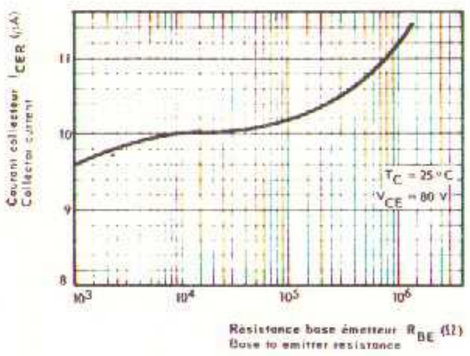
TENSION DE SATURATION COLLECTEUR EMETTEUR
EN FONCTION DU COURANT COLLECTEUR
COLLECTOR TO EMITTER SATURATION VOLTAGE
VERSUS COLLECTOR CURRENT



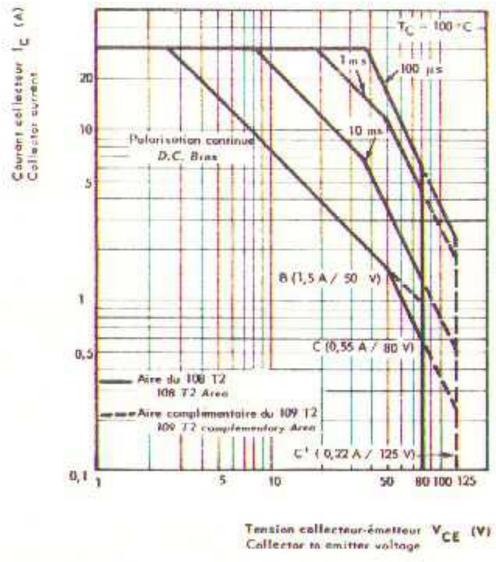
SCHEMA DE MESURE DES TEMPS DE COMMUTATION
SWITCHING TIME TEST CIRCUIT



COURANT COLLECTEUR EN FONCTION DE LA RESISTANCE BASE EMETTEUR
COLLECTOR CURRENT VERSUS
BASE TO EMITTER RESISTANCE

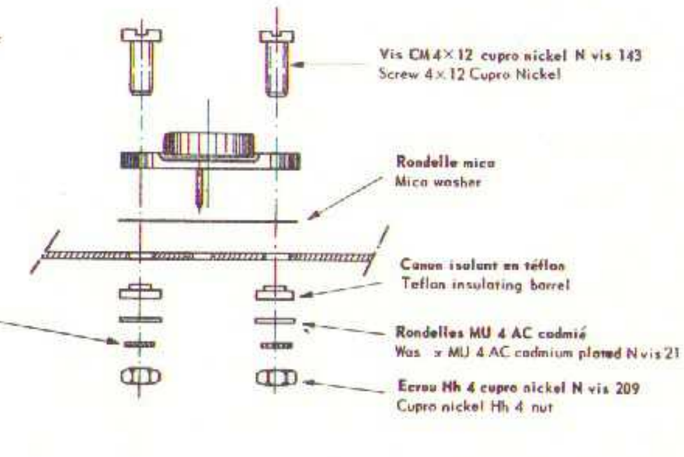


AIRE DE SECURITE (facteur de forme 1 %)
SAFE AREA (duty cycle 1 %)



EQUIPEMENT
MOUNTING HARDWARE

Ces dispositifs sont livrés avec l'équipement suivant :
Mounting hardware :



RCA linear integrated circuits

DC Amplifier

Monolithic Silicon

CA3000

File No. 121

- Designed for use in Communication, Telemetry, Instrumentation, and Data-Processing Equipment
- Balanced differential-amplifier configuration with controlled constant-current source to provide outstanding versatility
- Built-in temperature stability for operation from -55°C to +125°C
- Companion Application Note, ICAN 5030 "Applications of RCA CA3000 Integrated Circuit DC Amplifier" covers characteristics of different operating modes, frequency considerations, 10 Mc/s narrow band tuned amplifier design, crystal oscillator design, and many other application aids

HIGHLIGHTS

- Input Impedance . . . . . 195 kΩ typ.
- Voltage Gain. . . . . 37 dB typ.
- Common-Mode Rejection Ratio . . . 98 dB typ.
- Input Offset Voltage. . . . . 1.4 mV typ.
- Push-Pull Input and Output
- Frequency Capability
  DC to 30 Mc/s (with external C and R)
- Wide AGC Range. . . . . 90 dB typ.

APPLICATIONS

- Schmitt Trigger
- RC-Coupled Feedback Amplifier
- Mixer
- Comparator
- Modulator
- Crystal Oscillator
- Sense Amplifier

SCHEMATIC DIAGRAM

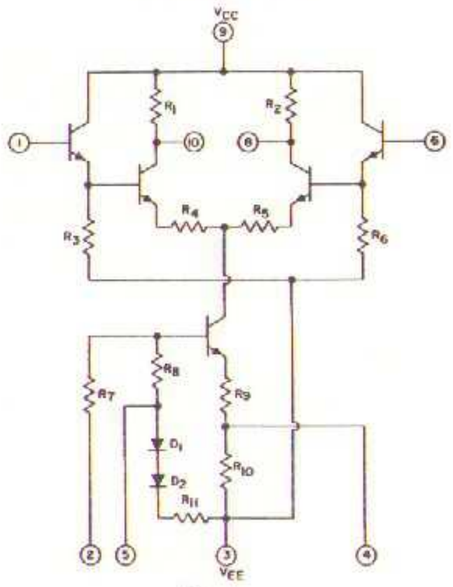
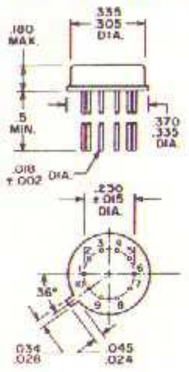


Fig. 1

DIMENSIONAL OUTLINE FOR CA3000



RADIO CORPORATION OF AMERICA
ELECTRONIC COMPONENTS AND DEVICES, HARRISON, N.J.

CA3000 6-66
Reprinted from Issue dated 2-66

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Indicated voltage limits for each terminal can be used under specified voltage conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2	+2	2	0
			3	-6
			6	0
			9	+6
2	-8	0	1	0
			3	-8
			6	0
			9	+6
3	-10	0	1	0
			2	0
			6	0
			9	+6
4	-8	0	1	0
			2	0
			6	0
			9	+6
5	-6	0	1	0
			2	0
			3	-6
			6	0
			9	+6
6	-2	+2	1	0
			2	0
			3	-6
			9	+6
7	NO CONNECTION			
8	0	+6	1	0
			2	0
			3	-6
			6	0
9	0	+10	1	0
			2	0
			3	-6
			6	0
10	0	+6	1	0
			2	0
			3	-6
			6	0
CASE	Internally Connected to Terminal No.3 (Substrate) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE	-55°C to +125°C
STORAGE-TEMPERATURE RANGE	-65°C to +200°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	+2 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	+2 V
MAXIMUM DEVICE DISSIPATION	300 mW

ELECTRICAL CHARACTERISTICS, at T_{FA} = 25°C, V_{CC} = +6V, V_{EE} = -6V, unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 & No.5 Not Connected Unless Specified		TEST CIRCUITS	LIMITS TYPE CA3000				TYPICAL CHARACTERISTICS CURVES
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}			4	-	1.4	8	mV	2
Input Offset Current	I_{IO}			5	-	1.2	10	μA	2
Input Bias Current	I_I			5	-	23	36	μA	3
Quiescent Operating Voltage	V_8 or V_{IO}	TERMINALS 4	5						
		NC	NC	7	-	2.6	-	V	6
		NC	VEE	7	-	4.2	-	V	6
		VEE	NC	7	-	-1.5	-	V	6
		VEE	VEE	7	-	0.6	-	V	6
Device Dissipation	P_T	NC	NC	7	-	30	-	mW	NONE
DYNAMIC CHARACTERISTICS									
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single-Ended Output f = 1 kc/s		9	28	32	-	dB	8
		Double-Ended Output f = 1 kc/s		9	-	37	-	dB	8
Bandwidth at -3 dB Point	BW			11	-	650	-	kc/s	10
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	f = 1 kc/s		9	-	6.4	-	V(P-P)	NONE
Common-Mode Rejection Ratio	CMR	f = 1 kc/s		13	80	98	-	dB	12
Single-Ended Input Impedance	Z_{IN}	f = 1 kc/s		15	70K	195K	-	Ω	14
Single-Ended Output Impedance	Z_{OUT}	f = 1 kc/s		17	5.5K	8K	10.5K	Ω	16
Total Harmonic Distortion	THD	f = 1 kc/s		19	-	0.2	5	%	18
AGC Range (Maximum Voltage Gain to Complete Cutoff)	AGC	f = 1 kc/s		20	80	90	-	dB	NONE

DEFINITIONS OF TERMS FOR CA3000

Total Harmonic Distortion

The ratio of the total rms voltage of all harmonics to the rms voltage of the Fundamental, expressed in per cent. This voltage is measured at either output terminal with respect to ground.

Input Offset Voltage

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Input Offset Current

The difference in the currents at the two input terminals.

Input Bias Current

The average value (one-half the sum) of the currents at the two input terminals.

Quiescent Operating Voltage

The dc voltage at either output terminal, with respect to ground.

DC Device Dissipation

The total power drain of the device with no signal applied and no external load current.

Common-Mode Voltage Gain

The ratio of the signal voltages developed between the two output terminals to the signal voltage applied to the two input terminals connected in parallel for ac.

Differential Voltage Gain — Single-Ended Input/Output

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground.

Common-Mode Rejection Ratio

The ratio of the full differential voltage gain to the common-mode voltage gain.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

Bandwidth at -3-dB Point (BW)

The frequency at which the voltage gain of the device is 3 dB below the voltage gain at a specifed lower frequency.

Maximum Output Voltage $V_{OUT(P-P)}$

The maximum peak-to-peak output-voltage swing, measured with respect to ground, which can be achieved without clipping of the signal waveform.

Single-Ended Input Impedance (Z_{IN})

The ratio of the change in input voltage to the change in input current measured at either input terminal with respect to ground.

Single-Ended Output Impedance (Z_{OUT})

The ratio of the change in output voltage to the change in output current measured at either output terminal with respect to ground.

STATIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3000

INPUT OFFSET VOLTAGE AND CURRENT vs TEMPERATURE

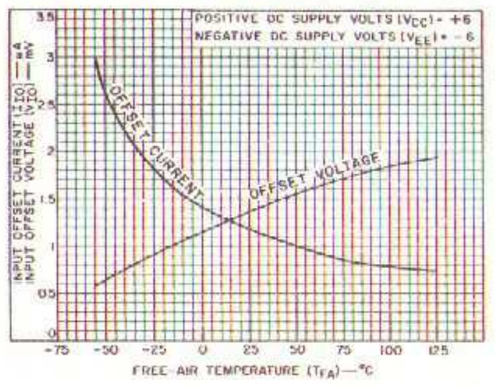


Fig. 2

INPUT BIAS CURRENT vs TEMPERATURE

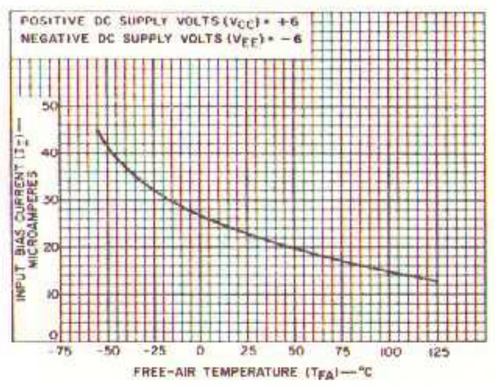
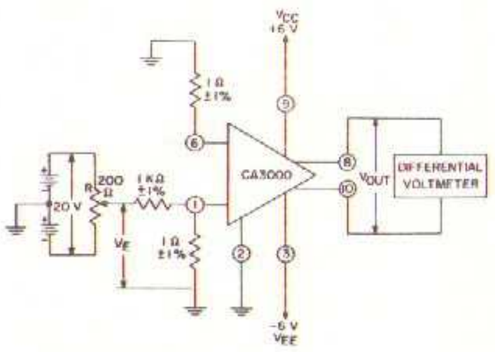


Fig. 3

INPUT OFFSET VOLTAGE TEST CIRCUIT



1. Adjust R for V_{OUT} (DC) = 0 ± 0.1 V.
2. Measure V_E and record Input Offset Voltage in mV;

$$V_{IO} = \frac{V_E}{1000}$$

Fig. 4

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

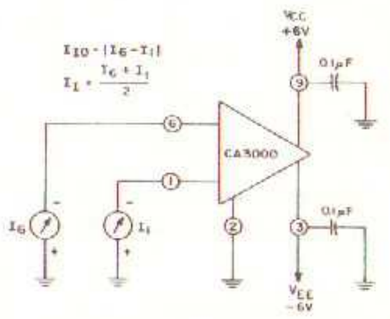


Fig. 5

STATIC CHARACTERISTICS AND TEST CIRCUIT FOR TYPE CA3000

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

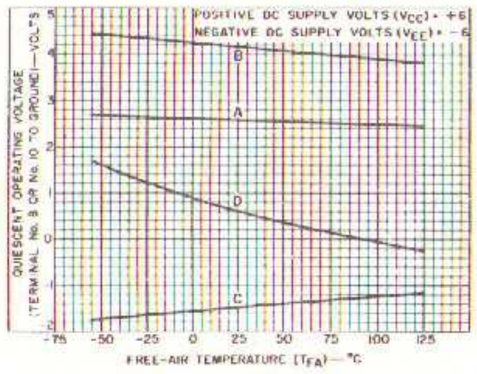
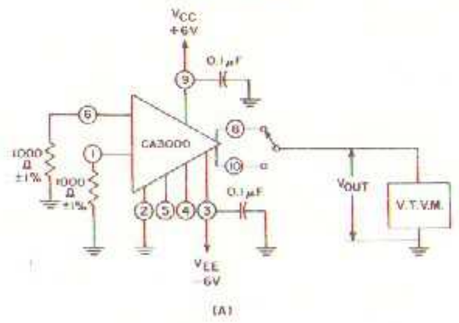


Fig.6

QUIESCENT OPERATING VOLTAGE AND DEVICE DISSIPATION TEST CIRCUIT



$P_T = V_{EE} I_3 + V_{CC} I_9$

I_3 = Direct Current out of Terminal No.3

I_9 = Direct Current into Terminal No.9

Fig.7

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT FOR TYPE CA3000

DIFFERENTIAL VOLTAGE GAIN vs TEMPERATURE

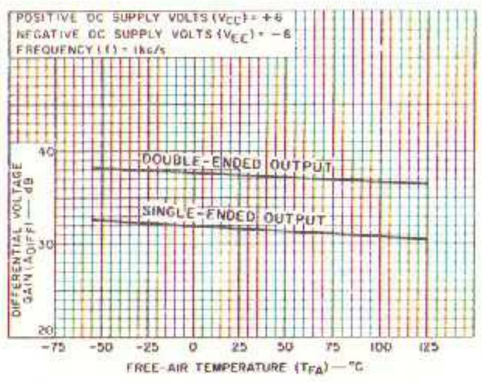
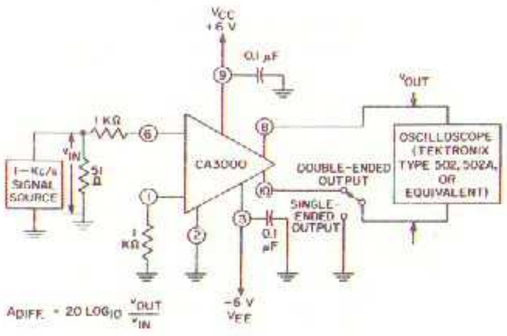


Fig.8

DIFFERENTIAL VOLTAGE GAIN AND MAXIMUM OUTPUT VOLTAGE SWING TEST CIRCUIT



$A_{DIFF} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$

Fig.9

DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3000

SINGLE-ENDED INPUT IMPEDANCE vs TEMPERATURE

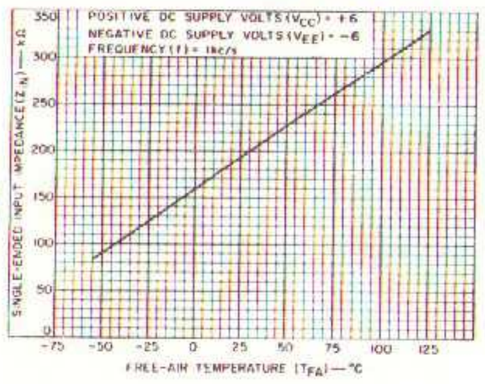


Fig.14

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

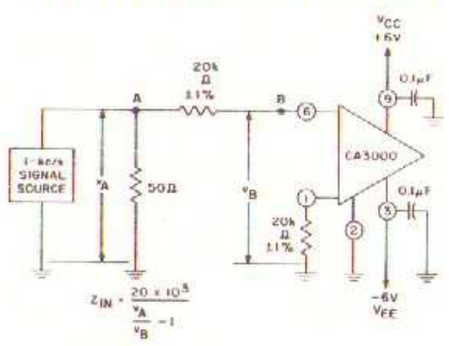


Fig.15

SINGLE-ENDED OUTPUT IMPEDANCE vs TEMPERATURE

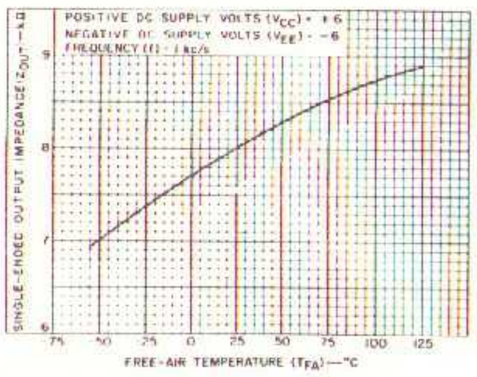
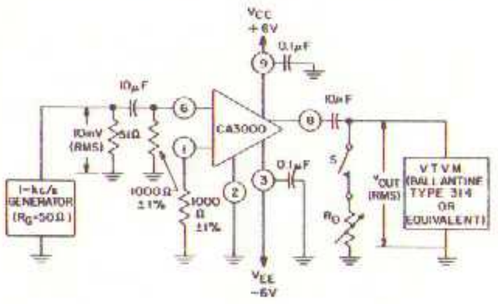


Fig.16

SINGLE-ENDED OUTPUT IMPEDANCE TEST CIRCUIT



1. With Switch S open, record reference voltage $V_{OUT(rms)}$.
2. Close Switch S, and adjust R_O until
$$V_{OUT} = \frac{\text{Reference Voltage}}{2}$$
3. Record value of R_O as Z_{OUT}.

Fig.17

DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3000

BANDWIDTH AT -3 dB POINT vs TEMPERATURE

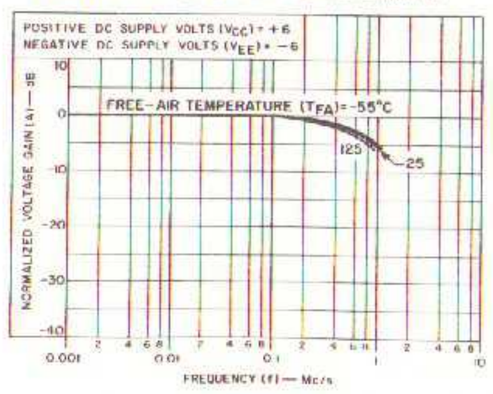
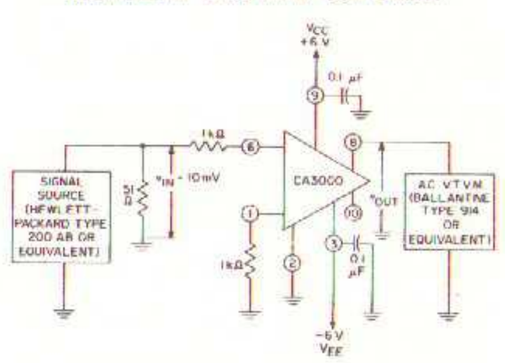


Fig.10

BANDWIDTH AT -3 dB POINT TEST CIRCUIT



1. Apply 1 kc/s, 10 mV(rms) input signal to set reference level.
2. Increase frequency (Keeping V_{IN} equal to 10 mV(rms)) until V_{OUT}/V_{IN} is 3 dB down from 1 kc/s reference level.
3. Record Bandwidth.

Fig.11

COMMON-MODE REJECTION RATIO vs TEMPERATURE

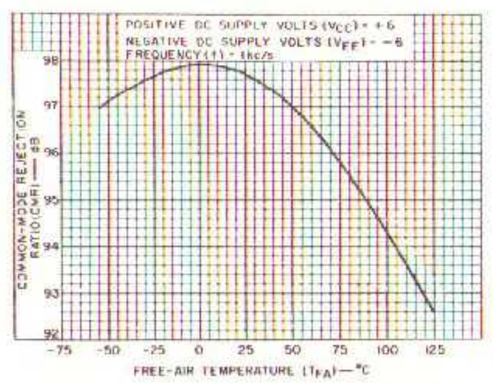
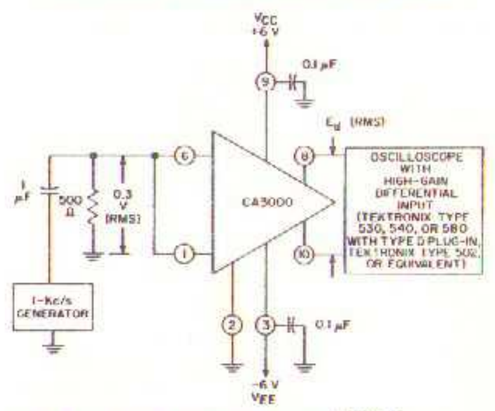


Fig.12

COMMON-MODE REJECTION RATIO TEST CIRCUIT



COMMON-MODE REJECTION RATIO (CMR) = $20 \log \frac{(A^*)(2)(0.3)}{E_d\,(RMS)}$

*A = SINGLE-ENDED VOLTAGE GAIN

Fig.13

DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3000

TOTAL HARMONIC DISTORTION vs TEMPERATURE

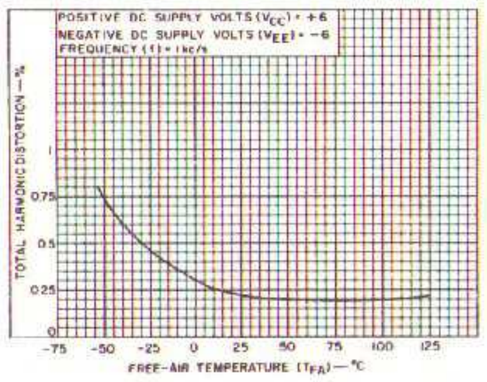


Fig.18

TOTAL HARMONIC DISTORTION TEST CIRCUIT

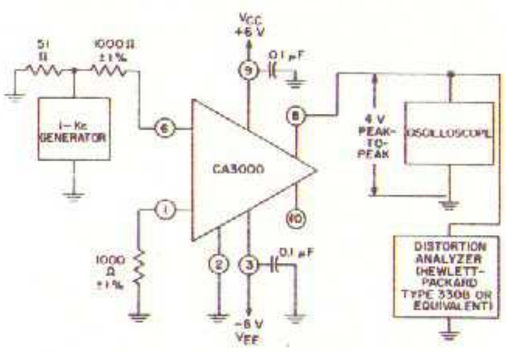


Fig.19

SINGLE-ENDED OUTPUT IMPEDANCE vs TEMPERATURE

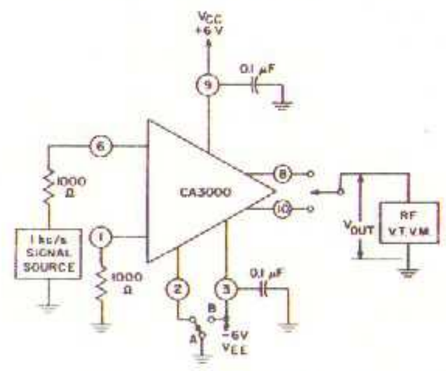
Fig.16

SINGLE-ENDED OUTPUT IMPEDANCE TEST CIRCUIT

1. With Switch S open, record reference voltage $V_{OUT(rms)}$.
2. Close Switch S, and adjust R_O until
$$V_{OUT} = \frac{\text{Reference Voltage}}{2}$$
3. Record value of R_O as Z_{OUT}.

Fig.17

AGC RANGE TEST CIRCUIT



AGC Range = $20 \log_{10} \frac{\text{A with S in Position A}}{\text{A with S in Position B}}$

Fig.20

RCA linear integrated circuits — General-Purpose Transistor Arrays

CA3018
CA3018A

Monolithic Silicon

File No. 338

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low-power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

TWO ISOLATED TRANSISTORS AND A DARLINGTON-CONNECTED TRANSISTOR PAIR

For Low-Power Applications at Frequencies from DC Through the the VHF Range

12-Lead TO-5 Style

APPLICATIONS

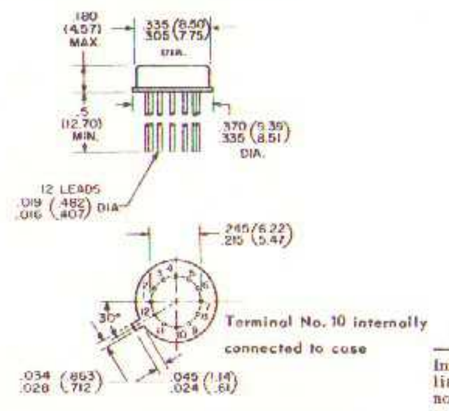
- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated-Circuit Transistor Array" for suggested Applications.

FEATURES

- Matched monolithic general purpose transistors
- H_{FE} matched ± 10%
- V_{BE} matched ± 2 mV CA3018A (± 5mV CA3018)
- Operation from DC to 120 MHz
- Wide operating current range
- CA3018A performance characteristics controlled from 10 μ A to 10mA
- Low noise figure - - 3.2 dB typical at 1KHz
- Full military temperature range capability (-55 to + 125°C)

DIMENSIONAL OUTLINE

Dimensions In Inches and millimeters



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.

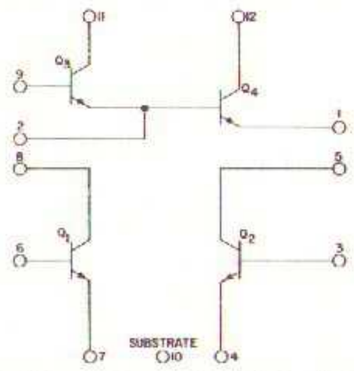


Fig. 1 - Schematic Diagram for CA3018 and CA3018A

Maximum Ratings, Absolute-Maximum Values, at TA=25°C

	CA3018	CA3018A	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	450	450	mW
Derate at 5 mW/°C for T_A > 85°C			
Temperature Range:			
Operating	-55 to + 125	-55 to + 125	°C
Storage	-65 to + 200	-65 to + 200	°C

The following ratings apply for each transistor in the device:

	CA3018	CA3018A	
Collector-to-Emitter Voltage, V_{CEO}	15	15	V
Collector-to-Base Voltage, V_{CBO}	20	30	V
Collector-to-Substrate Voltage, V_{CIO}*	20	40	V
Emitter-to-Base Voltage, V_{EBO}	5	5	V
Collector Current, I_C	50	50	mA

*The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. *The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

Characteristics apply for each transistor in the CA3018 and CA3018A as specified.

ELECTRICAL CHARACTERISTICS at T_A = 25°C	SYMBOLS	SPECIAL TEST CONDITIONS	CA3018 LIMITS Min.	CA3018 LIMITS Typ.	CA3018 LIMITS Max.	CA3018A LIMITS Min.	CA3018A LIMITS Typ.	CA3018A LIMITS Max.	Units	CHARACTERISTICS CURVES Fig.
STATIC CHARACTERISTICS										
Collector-Cutoff Current	I_{CBO}	V_{CB}=10V, I_E=0	-	0.002	100	-	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE}=10V, I_B=0		See Curve	5	-	See Curve	0.5	μA	3
Collector-Cutoff Current Darlington Pair	I_{CEO}	V_{CE}=10V, I_B=0	-	-	-	-	-	5	μA	-
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	15	24	-	15	24	-	V	-
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10μA, I_E=0	20	60	-	30	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=10μA, I_C=0	5	7	-	5	7	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C=10μA, I_{C1}=0	20	60	-	40	60	-	V	-
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B=1mA, I_C=10mA	-	0.23	-	-	0.23	0.5	V	-
Static Forward Current Transfer Ratio	h_{FE}	V_{CE}=3V, I_C=10mA / I_C=1mA / I_C=10μA	- / 30 / -	100 / 100 / 54	- / - / -	50 / 60 / 30	100 / 100 / 54	- / - / -	-	4
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		V_{CE}=3V, I_{C1}=I_{C2}=1mA	0.9	0.97	-	0.9	0.97	-	-	4
Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	h_{FED}	V_{CE}=3V, I_C=1mA / I_C=100μA	1500 / -	5400 / -	- / -	2000 / 1000	5400 / 2000	- / -	-	5
Base-to-Emitter Voltage	V_{BE}	V_{CE}=3V, I_E=1mA / I_E=10mA	- / -	0.715 / 0.800	- / -	0.600 / -	0.715 / 0.800	0.800 / 0.900	V	6
Input Offset Voltage	$\lvert V_{BE_1} - V_{BE_2} \rvert$	V_{CE}=3V, I_C=1mA	-	0.48	5	-	0.48	2	mV	6,8
Temperature Coefficient: Base-to-Emitter Voltage Q_1,Q_2	$\lvert \frac{\Delta V_{BE}}{\Delta T} \rvert$	V_{CE}=3V, I_E=1mA	-	-1.9	-	-	-1.9	-	mV/°C	7
Base-(Q3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{BED} (V_{Q-1})	V_{CE}=3V / I_E=10mA / I_E=1mA	- / -	1.46 / 1.32	- / -	- / 1.10	1.46 / 1.32	1.60 / 1.50	V	9
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	$\lvert \frac{\Delta V_{BED}}{\Delta T} \rvert$	V_{CE}=3V, I_E=1mA	-	4.4	-	-	4.4	-	mV/°C	10
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\lvert \frac{V_{BE_1} - V_{BE_2}}{\Delta T} \rvert$	V_{CC}=+6V, V_{EE}= 6V, I_{C1}=I_{C2}=1mA	-	10	-	-	10	-	μV/°C	-

CA3018, CA3018A — File No. 338

ELECTRICAL CHARACTERISTICS, (CONT'D)

DYNAMIC CHARACTERISTICS										
Low Frequency Noise Figure	NF	f=1 Kilz, V_{CE}=3V, I_C=100μA Source resistance=1 KΩ	-	3.25	-	-	3.25	-	dB	11(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward Current-Transfer Ratio	h_{fe}	f=1kHz, V_{CE}=3V, I_C=1mA	-	110	-	-	110	-	-	12
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	-	3.5	-	KΩ	12
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	-	15.6	-	μmho	12
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-	1.8×10^{-4}	-	-	12
Admittance Characteristics:										
Forward Transfer Admittance	Y_{fe}	f=1MHz, V_{CE}=3V, I_C=1mA	-	31-j1.5	-	-	31-j1.5	-	mmho	13
Input Admittance	Y_{ie}		-	0.3+j0.04	-	-	0.3+j0.04	-	mmho	14
Output Admittance	Y_{oe}		-	0.001+j0.03	-	-	0.001+j0.03	-	mmho	15
Reverse Transfer Admittance	Y_{re}		See Curve			See Curve			mmho	16
Gain-Bandwidth Product	f_t	V_{CE}=3V, I_C=3mA	300	500	-	300	500	-	MHz	17
Emitter-to-Base Capacitance	C_{EB}	V_{EB}=3V, I_E=0	-	0.6	-	-	0.6	-	pF	-
Collector-to-Base Capacitance	C_{CI}	V_{CO}=3V, I_C=0	-	0.58	-	-	0.58	-	pF	-
Collector-to-Substrate Capacitance	C_{CI}	V_{CI}=3V, I_C=0	-	2.8	-	-	2.8	-	pF	-

STATIC CHARACTERISTICS

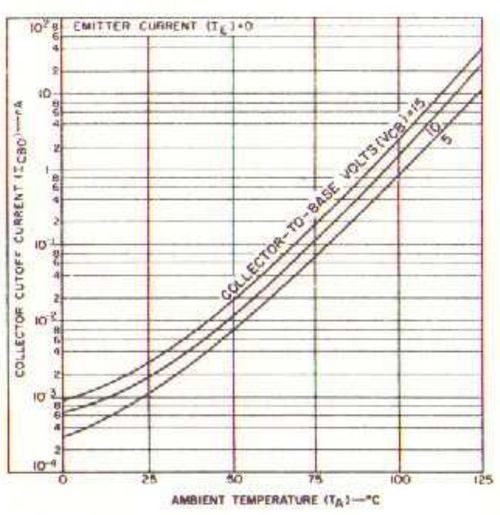


Fig.2 - Typical Collector-To-Base Cutoff Current vs Ambient Temperature for Each Transistor.

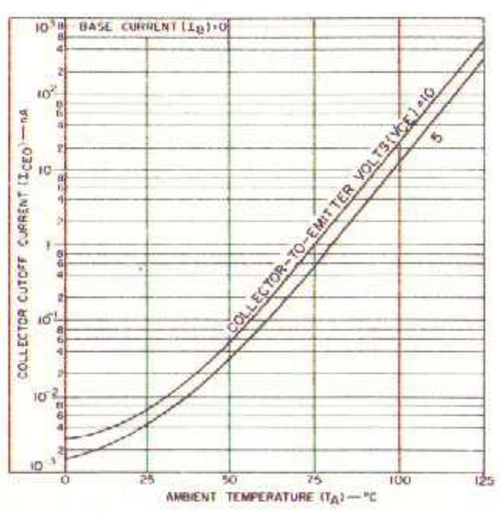


Fig.3 - Typical Collector-To-Emmiter Cutoff Current vs Ambient Temperature for Each Transistor.

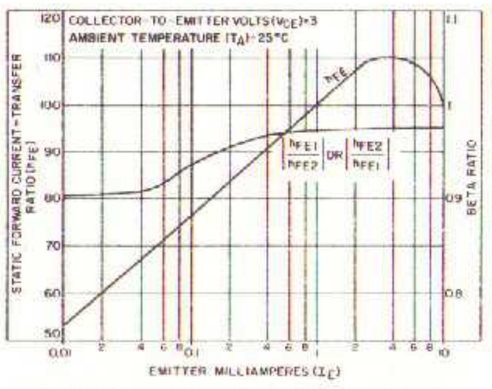


Fig.4 - Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q, and Q_2 vs Emitter Current.

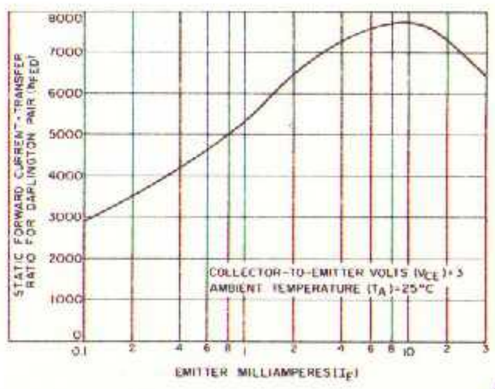


Fig.5 - Typical Static Forward Current - Transfer Ratio for Darlington-connected Transisters Q_3 and Q_4 vs Emitter Current.

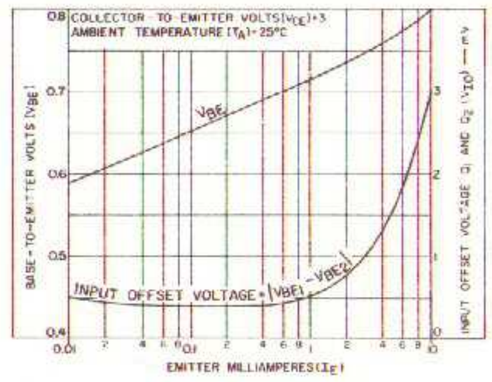


Fig.6 - Typical Static Base-to-Emitter Voltage Characteristic and Input Offset Voltage for Q_1 and Q_2 vs Emitter Current.

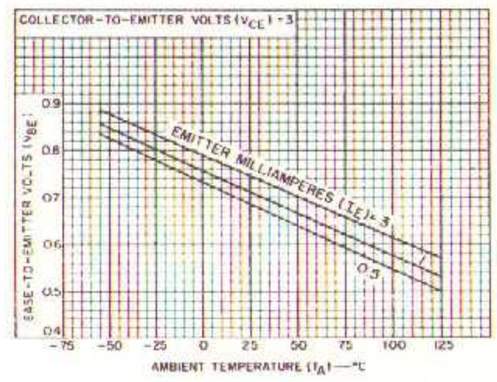


Fig.7 - Typical Base-To-Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature

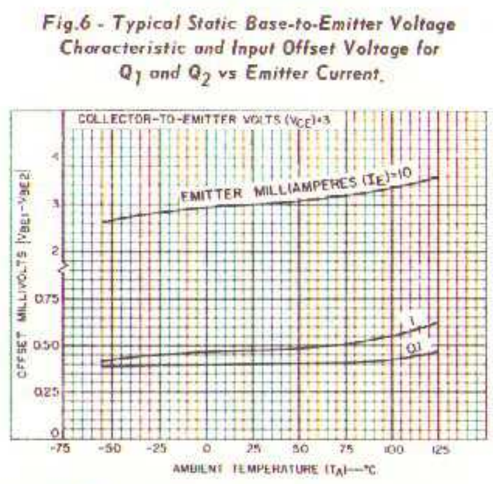


Fig.8 - Typical Offset Voltage Characteristic vs Ambient Temperature

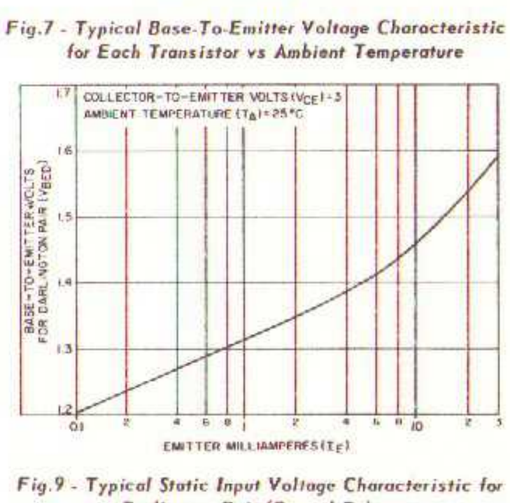


Fig.9 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Emitter Current

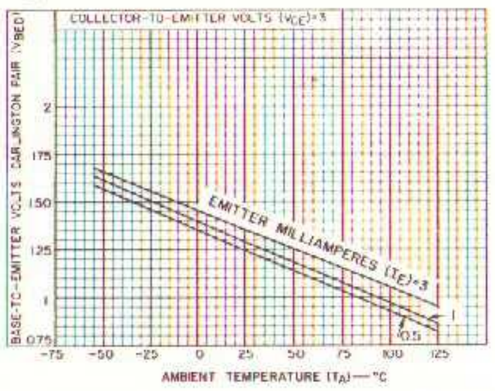


Fig. 10 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Ambient Temperature.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

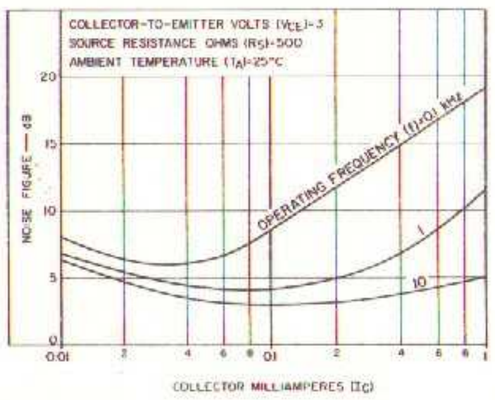


Fig. 11(a) - Noise Figure vs Collector Current, R_S = 500 Ω.

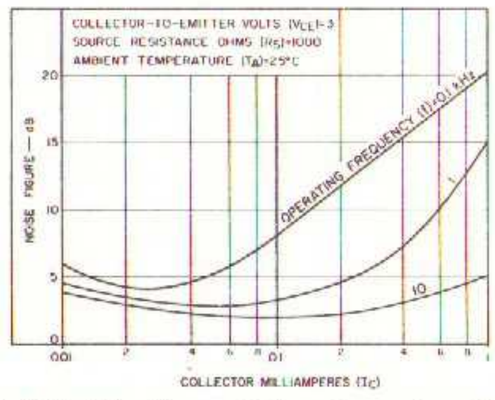


Fig. 11(b) - Noise Figure vs Collector Current, R_S = 1 KΩ.

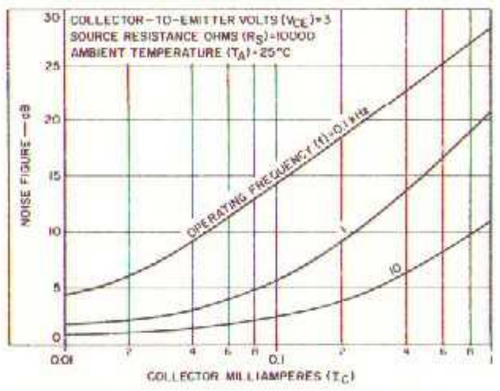


Fig. 11(c) - Noise Figure vs Collector Current, R_S = 10 KΩ.

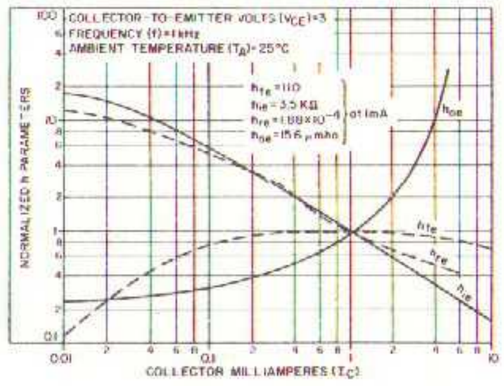


Fig. 12 - Forward Current-Transfer Ratio (h_{fe}), Short-Circuit Input Impedance (h_{ie}), Open-Circuit Output Impedance (h_{oe}), and Open-Circuit Reverse Voltage-Transfer Ratio (h_{re}) vs Collector Current

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

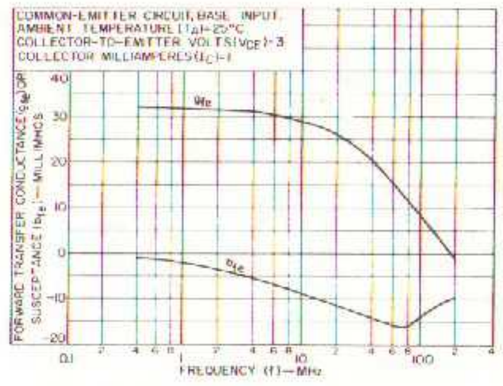


Fig. 13 - Forward Transfer Admittance (Y_{fe})

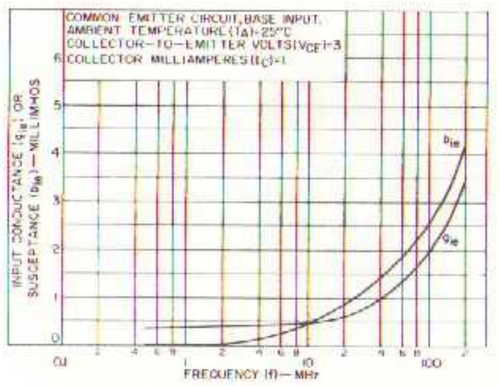


Fig. 14 - Input Admittance (Y_{ie})

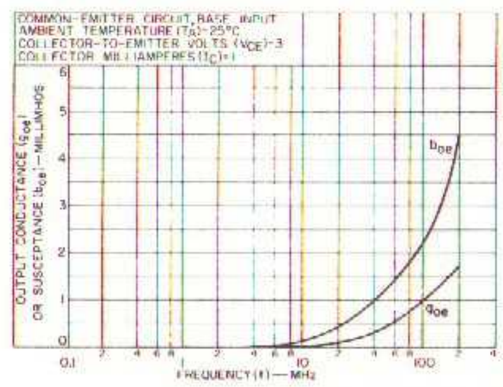


Fig. 15 - Output Admittance (Y_{oe})

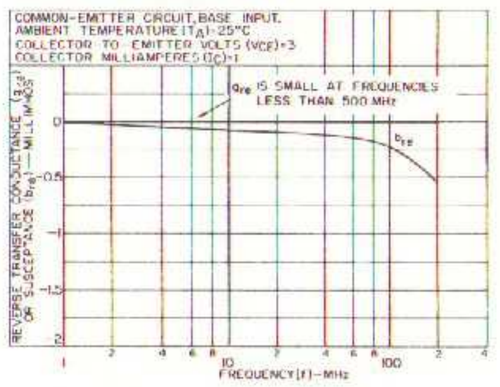


Fig. 16 - Reverse Transfer Admittance (Y_{re})

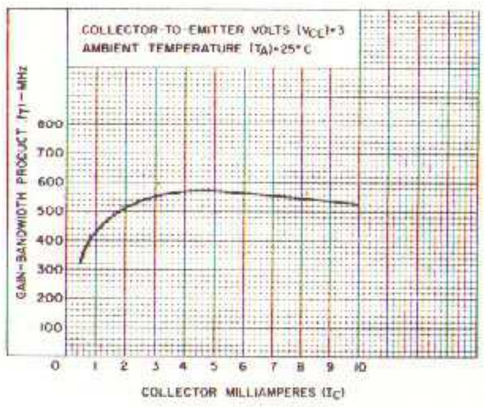


Fig. 17 - Typical Gain-Bandwidth Product (f_T) vs Collector Current

Circuit converts two analog quantities to frequency or period

Circuits that produce output signals with a frequency or period proportional to one or more analog quantities find widespread use in control and measurement systems.

One such circuit for converting two analog quantities, X and Y, into an output signal that has a frequency $f = kY/X$ or a period $T = kX/Y$ is shown in simplified form in Fig. 1. The circuit inputs, derived from the analog quantities, are current I and voltage V.

In operation, the input current I charges capacitor C through resistor R_1. When the potential of point M reaches that of point N, the amplifier output, initially at some positive voltage $+E_1$, switches to a negative voltage $-E_2$. This forward biases diode D and switches transistor Q on.

As a result, point N abruptly drops very close to ground potential, and C discharges through the forward biased diode. When the discharge of C again brings point M to the same potential as N, the amplifier output switches back to $+E_1$. This reverse biases D and turns Q off, so the circuit is prepared for the next cycle. The amplifier, therefore functions as a dual-level voltage comparator. A necessary condition for operation of the circuit is that the discharge time for C be very short compared to the charging time.

It is clear from the preceding description that the duration of one cycle is proportional to the voltage V and inversely proportional to the current I, or

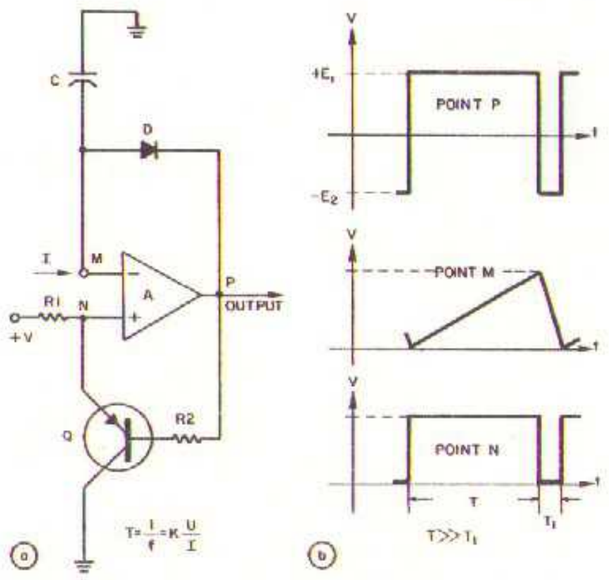
$$T = 1/f = k(V/I).$$

So the circuit converts either V/I to period or I/V to frequency. If the current I is held constant, then $T = kV$. Similarly if V is constant, $f = kI$.

Under the condition $T >> T_1$ (Fig. 1b), conversion error in the circuit arises only from the finite value of V_{CE} for the switching transistor. Likewise, conversion stability depends only on the stability of the V_{CE} value. If a transistor is used that has a V_{CE} less than 10 mV and good high temperature stability, the conversion error of the circuit can be less than 0.1%.

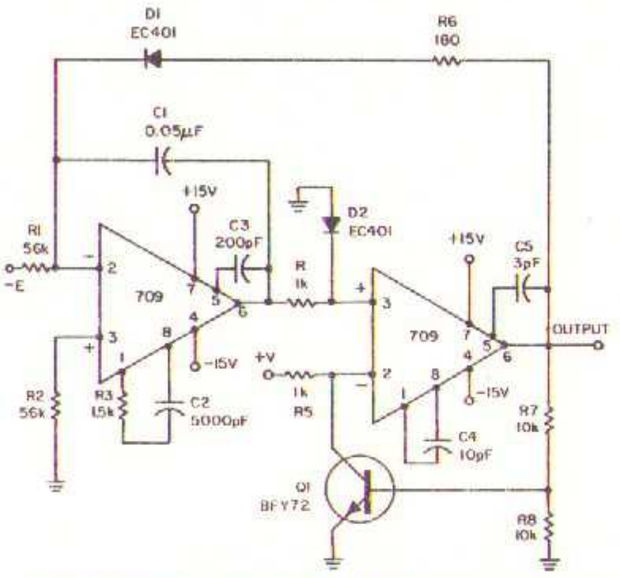
A complete circuit of this type, suitable for practical applications, is shown in Fig. 2. Measurements have shown it to be stable, accurate and linear, with errors on the order of 0.1% for input quantity variations of more than 40 dB.

IDEA FOR DESIGN



1. Amplifier A functions as a dual-level comparator (a). It compares the voltages at points M and N, and switches the output level at P each time they are equal (b).

ELECTRONIC DESIGN 6, March 15, 1969



2. Two monolithic operational amplifiers are used in a practical version of the converter.

RCA linear integrated circuits

Multipurpose Wide-Band Power Amplifiers

Monolithic Silicon

CA3020
CA3020A

File No. 339

The RCA-CA3020 and CA3020A are Integrated-Circuit, Multistage, Multipurpose, Wide-Band Power Amplifiers on a single monolithic silicon chip. They employ a highly versatile and stable direct-coupled circuit configuration featuring wide frequency range, high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020 and CA3020A extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The CA3020 and CA3020A are particularly suited for service as Class B power amplifiers. The CA3020A can provide a maximum power output of 1 watt from a 12-volt DC supply with a typical power gain of 75 dB. The CA3020 provides 0.5 watt power output from a 9-volt supply with the same power gain.

These types are supplied in hermetically sealed, TO-5 style 12-lead packages.

SCHEMATIC DIAGRAM FOR CA3020 AND CA3020A

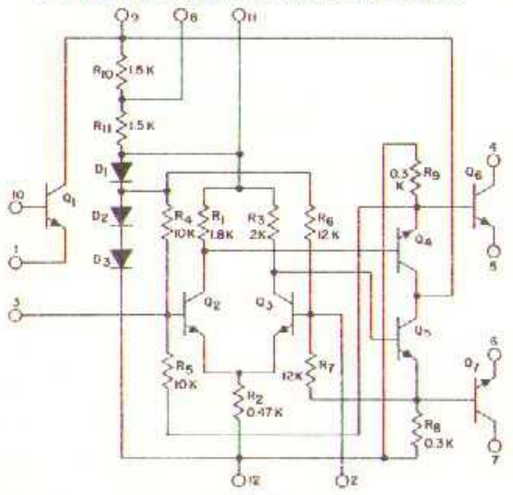


Fig. 1

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ± 30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

MULTIPURPOSE WIDE-BAND POWER AMPLIFIERS

For Military, Industrial, and Commercial Equipment at Frequencies up to 8 MHz

12-Lead TO-5

FEATURES

- High power output - class B amplifier --
  CA3020 .... 0.5 watt typ. at V_{CC} = +9V
  CA3020A ... 1.0 watt typ. at V_{CC} = +12V
- Wide frequency range --
  Up to 8 MHZ with resistive loads
- High power gain ..... 75db typ.
- Single power supply for class B operation with transformer --
  CA3020 ..... 3 to 9V
  CA3020A ..... 3 to 12V
- Built-in temperature-tracking voltage regulator provides stable operation over -55°C to +125°C temperature range

APPLICATIONS

- AF power amplifiers for portable and fixed sound and communications systems
- Servo-control amplifiers
- Wide-band linear mixers
- Video power amplifiers
- Transmission-line driver amplifiers (balanced and unbalanced)
- Fan-in and fan-out amplifiers for computer logic circuits
- Lamp-control amplifiers
- Motor-control amplifiers
- Power multivibrator
- Power switches
- Companion Application Note, ICAN 5766 "Application of CA3020 and CA3020A Integrated Circuit Multipurpose Wide-Band Power Amplifiers."

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS CA3020			LIMITS CA3020A			UNITS
		CIRCUIT AND PROCEDURE FIG.	DC SUPPLY VOLTAGE V_{CC1}	DC SUPPLY VOLTAGE V_{CC2}	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Collector-to-Emitter Breakdown Voltage, Q_6 & Q_7 at 10 mA	$V_{(BR)CEO}$	-	-	-	18	-	-	25	-	-	V
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1 mA	$V_{(BR)CEO}$	-	-	-	10	-	-	10	-	-	V
Idle Currents, Q_6 & Q_7	I_4 IDLE I_7 IDLE	8	9.0	2.0	-	5.5	-	-	5.5	-	mA
Peak Output Currents, Q_6 & Q_7	I_4PK I_7PK	8	9.0	2.0	140	-	-	180	-	-	mA
Cutoff Currents, Q_6 & Q_7	I_4 CUTOFF I_7 CUTOFF	8	9.0	2.0	-	-	1.0	-	-	1.0	mA
Differential Amplifier Current Drain	I_{CC1}	8	9.0	9.0	6.3	9.4	12.5	6.3	9.4	12.5	mA
Total Current Drain	I_{CC1} + I_{CC2}	8	9.0	9.0	8.0	21.5	35.0	14.0	21.5	30.0	mA
Differential Amplifier Input Terminal Voltages	V_2 V_3	8	9.0	2.0	-	1.11	-	-	1.11	-	V
Regulator Terminal Voltage	V_{11}	8	9.0	2.0	-	2.35	-	-	2.35	-	V
Q, Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	-	10.0	-	-	-	100	-	-	100	μA
Emitter-to-Base	I_{EBO}		3.0	-	-	-	0.1	-	-	0.1	
Collector-to-Base	I_{CBO}		3.0	-	-	-	0.1	-	-	0.1	
Forward Current Transfer Ratio, Q_1 at 3 mA	h_{FE1}	-	6.0	-	30	75	-	30	75	-	
Bandwidth at -3 dB Point	BW	9	6.0	6.0	-	8	-	-	8	-	MHz
Maximum Power Output	$P_{O(MAX)}$	10	6.0	6.0	200	300[a]	-	200	300[a]	-	mW
			9.0	9.0	400	550[a]	-	400	550[a]	-	
			9.0	12.0	-	-	-	800	1000[b]	-	
Sensitivity for P_{OUT} = 400 mW	e_{IN}	10	9.0	9.0	-	35[a]	55	-	-	-	mV
Sensitivity for P_{OUT} = 800 mW	e_{IN}	10	9.0	12.0	-	-	-	-	50[b]	100	mV
Input Resistance Terminal 3 to Ground	R_{IN3}	11	6.0	6.0	-	1000	-	-	1000	-	Ω
Junction to Case Thermal Resistance	θ_{J-C}	-	-	-	-	-	60	-	-	60	°C/W

a R_{CC} = 130 Ω

b R_{CC} = 200 Ω

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:

WITHOUT HEAT SINK	WITH HEAT SINK
At T_A = 25°C ..... 1 W	At T_C = 25°C ..... 2 W
Above T_A = 25°C ..... derate linearly 6.7 mW/°C	At T_C = 25°C to T_C = 55°C ..... 2 W
	Above T_C = 55°C .. derate linearly 16.7 mW/°C

TEMPERATURE RANGE:

Operating ..... -55°C to +125°C
Storage ..... -65°C to +200°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 12 is 0 to +10 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		*	*	*	*	*	*	*	▲ 0 -10/-12	+3 Note 1	*	+10 0
2			*	*	*	*	*	*	*	*	*	+2 -2
3				*	*	*	*	*	*	*	*	+2 -2
4					▲ +18/+25 0	*	*	*	*	*	*	▲ +18/+25 0
5						*	*	*	*	*	*	+3 Note 2
6							▲ 0 -18/-25	*	*	*	*	+3 Note 2
7								*	*	*	*	▲ +18/+25 0
8									Note 3	*	*	Note 3 0
9										+10 0	Note 1 0	+10/+12 0
10											*	+10 0
11												*
12												REF. SUBSTRATE

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	20
2	-	-
3	-	-
4	300	-
5	-	300
6	-	300
7	300	-
8	-	-
9	20	-
10	1	-
11	20	-
12	-	-

Note 1: This voltage is established by the maximum current rating.

Note 2: The emitters of Q_6 and Q_7 may be returned to a negative voltage supply through emitter resistors. Current into terminal No.9 should not be exceeded and the total device dissipation should not be exceeded.

Note 3: Terminal No.8 may be connected to terminals Nos.9, 11, or 12.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

▲ Higher value is for CA3020A.

TYPICAL AUDIO AMPLIFIER CIRCUIT UTILIZING THE CA3020 OR CA3020A AS AN AUDIO PREAMPLIFIER AND CLASS B POWER AMPLIFIER

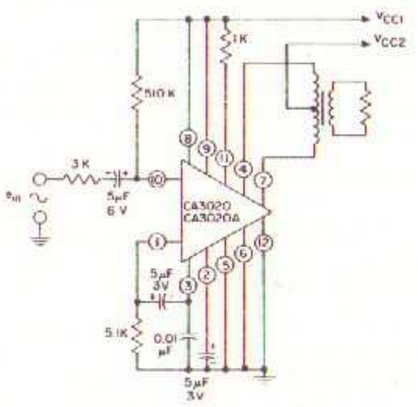


Fig.2

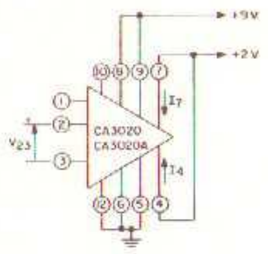
TYPICAL PERFORMANCE DATA*

An External Radiator is Recommended for High Ambient Temperature Operation

CHARACTERISTICS	SYMBOLS	CA3020	CA3020A	UNITS
Power Supply Voltage	V_{CC_1}	9.0	9.0	V
	V_{CC_2}	9.0	12.0	
Zero Signal Current Diff. Ampl.	I_{CC_1}	15	15	mA
Zero Signal Current Output Ampl.	I_{CC_2}	24	24	mA
Maximum Signal Current Diff. Ampl.	I_{CC_1}	16	16.6	mA
Maximum Signal Current Output Ampl.	I_{CC_2}	125	140	mA
Maximum Power Output at THD = 10%	Po	550	1000	mW
Sensitivity	e_{IN}	35	45	mV
Power Gain	G_P	75	75	dB
Input Resistance	R_{IN}	55	55	kΩ
Efficiency	η	45	55	%
Signal-to-Noise Ratio	S/N	70	66	dB
THD at 150 mW level		3.1	3.3	%
Test Signal Frequency from 600Ω Generator		1000	1000	Hz
Equivalent Collector-to-Collector Load Resistance	R_{CC}	130	200	Ω

* Refer to Figs.8 through 12 for Measurement and Symbol Information.

TYPICAL TRANSFER CHARACTERISTICS



a. Test Setup

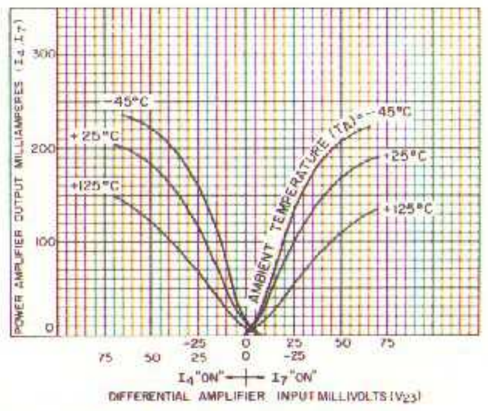
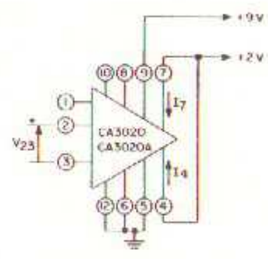


Fig.3 b. Characteristics with R_{10} shorted out



a. Test Setup

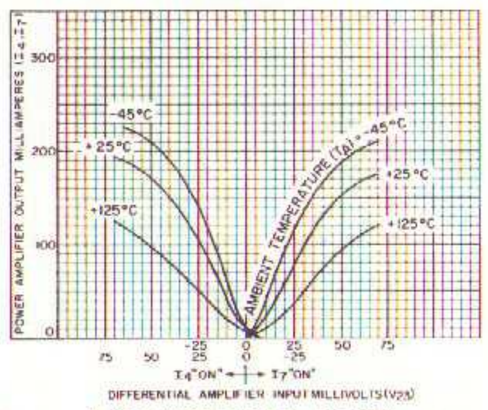
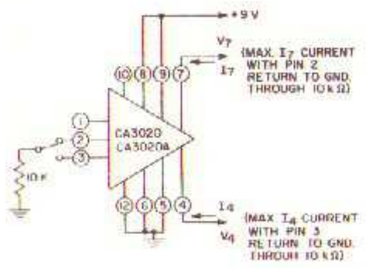


Fig.4 b. Characteristics with R_{10} in circuit

"MINIMUM DRIVE" TYPICAL CURRENT-VOLTAGE SATURATION CURVE



a. Test Setup

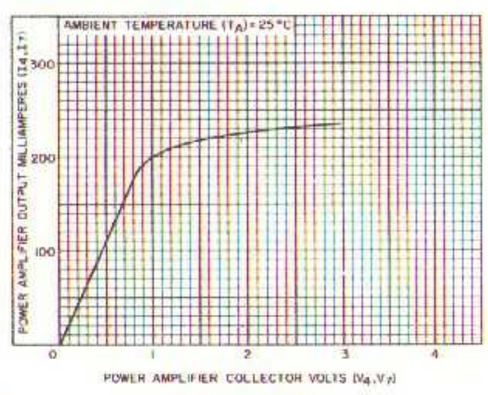
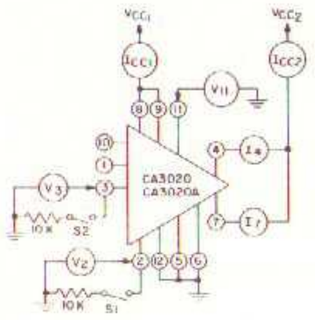


Fig.5 b. Characteristic

STATIC CURRENT AND VOLTAGE TEST CIRCUIT

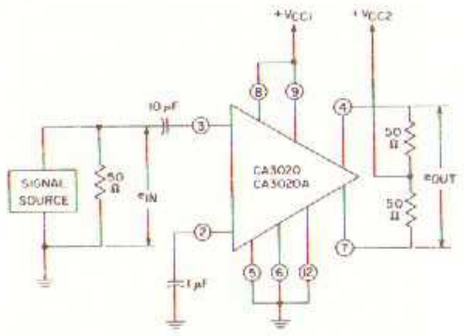


CURRENTS OR VOLTAGES	S1	S2
$I_{4\text{-IDLE}}$	open	open
$I_{7\text{-IDLE}}$	open	open
$I_{4\text{-PEAK}}$	open	close
$I_{7\text{-PEAK}}$	close	open
$I_{4\text{-CUTOFF}}$	close	open
$I_{7\text{-CUTOFF}}$	open	close

CURRENTS OR VOLTAGES	S1	S2
I_{CC1}	open	open
I_{CC2}	open	open
V_2	open	open
V_3	open	open
V_{11}	open	open

Fig.8

MEASUREMENT OF BANDWIDTH AT -3 dB POINTS

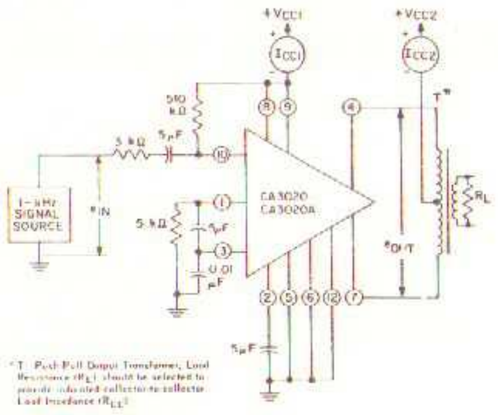


PROCEDURES:

1. Apply desired value of V_{CC_1} and V_{CC_2}
2. Apply 1 kHz input signal and adjust for e_{IN} = 5 mV (rms)
3. Record the resulting value of e_{OUT} in dB (reference value)
4. Vary input-signal frequency, keeping e_{IN} constant at 5 mV, and record frequencies above and below 1 kHz at which e_{OUT} decreases 3 dB below reference value.
5. Record bandwidth as frequency range between -3 dB points.

Fig.9

MEASUREMENTS OF ZERO-SIGNAL DC CURRENT DRAIN, MAXIMUM-SIGNAL DC CURRENT DRAIN, MAXIMUM POWER OUTPUT, CIRCUIT EFFICIENCY, SENSITIVITY, AND TRANSDUCER POWER GAIN



PROCEDURES:

Zero-Signal DC Current Drain

1. Apply desired Value of V_{CC_1} and V_{CC_2} and reduce e_{IN} to 0V
2. Record resulting values of I_{CC_1} and I_{CC_2} in mA as Zero-Signal DC Current Drain.

Fig.10

Maximum-Signal DC Current Drain, Maximum Power Output, Circuit Efficiency, Sensitivity, and Transducer Power Gain

1. Apply desired value of V_{CC_1} and V_{CC_2} and adjust e_{IN} to the value at which the Total Harmonic Distortion in the output of the amplifier = 10%
2. Record resulting value of I_{CC_1} and I_{CC_2} in mA as Maximum-Signal DC Current Drain
3. Determine resulting amplifier power output in watts and record as Maximum Power Output (P_{OUT})
4. Calculate Circuit Efficiency (η) in % as follows:

$$\eta = 100\,\frac{P_{OUT}}{V_{CC_1}I_{CC_1} + V_{CC_2}I_{CC_2}}$$

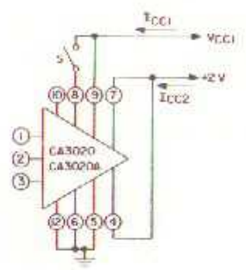
where P_{OUT} is in watts, V_{CC_1} and V_{CC_2} are in volts, and I_{CC_1} and I_{CC_2} are in amperes.

5. Record value of e_{IN} in mV (rms) required in Step 1 as Sensitivity (e_{IN})
6. Calculate Transducer Power Gain (G_p) in dB as follows:

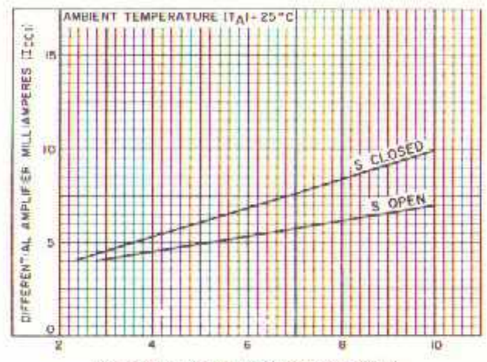
$$G_p = 10\log_{10}\frac{P_{OUT}}{P_{IN}}$$

where P_{IN} (in mW) = $\dfrac{e_{IN}^2}{3000 + R_{IN(10)}}$

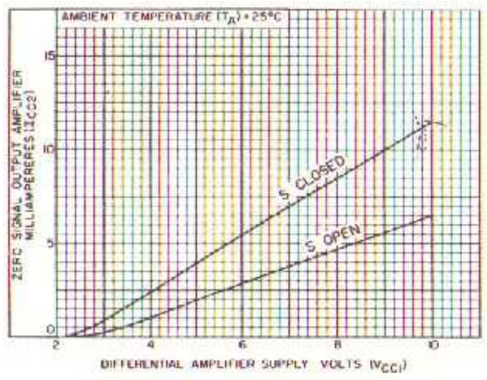
ZERO SIGNAL AMPLIFIER CURRENT vs DIFFERENTIAL AMPLIFIER SUPPLY VOLTAGE



a. Test Setup



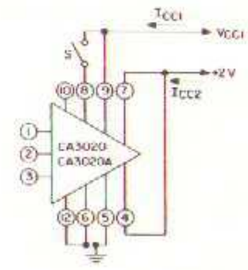
b. Differential Amplifier Characteristics



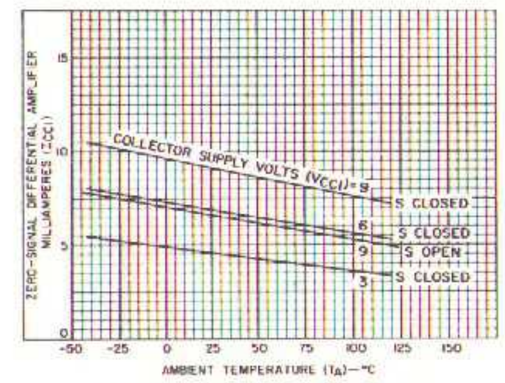
c. Output Amplifier Characteristics

Fig.6

ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE

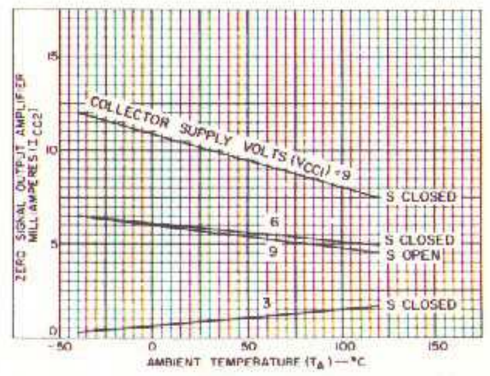


a. Test Setup



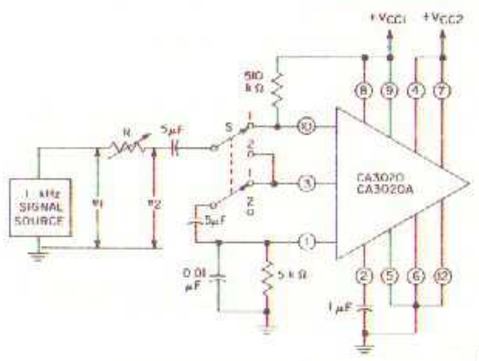
b. Differential Amplifier Characteristics

Fig.7



c. Output Amplifier Characteristics

MEASUREMENT OF INPUT RESISTANCE



PROCEDURES:

Input Resistance Terminal 10 to Ground ($R_{IN_{10}}$)

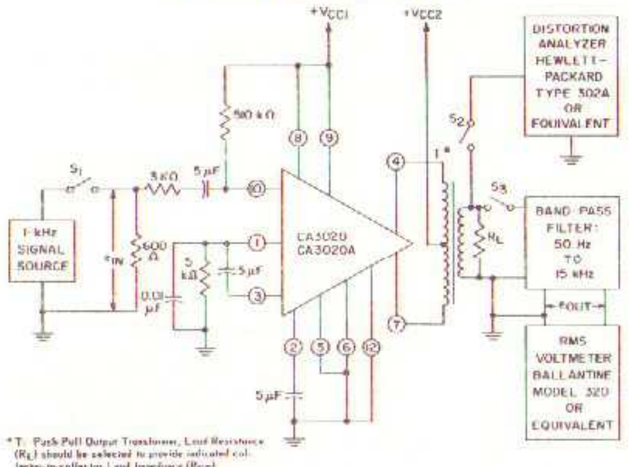
1. Apply desired value of V_{CC_1} and V_{CC_2} and set S in Position 1
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as $R_{IN_{10}}$

Input Resistance Terminal 3 to Ground (R_{IN_3})

1. Apply desired value of V_{CC_1} and V_{CC_2} set S in Position 2
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as R_{IN_3}

Fig.11

MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION



PROCEDURES:

Signal-to-Noise Ratio

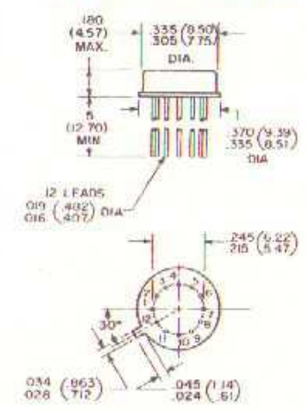
1. Close S_1 and S_3, open S_2
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for an amplifier output of 150mW and record resulting value of E_{OUT} in dB as e_{OUT_1} (reference value)
4. Open S_1 and record resulting value of e_{OUT} in dH as e_{OUT_2}
5. Signal-to-Noise Ratio (S/N) = $20\log_{10}\dfrac{e_{OUT_1}}{e_{OUT_2}}$.

Total Harmonic Distortion

1. Close S_1 and S_2; open S_3
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for desired level amplifier output power
4. Record Total Harmonic Distortion (THD) in %

Fig.12

DIMENSIONAL OUTLINE



DIMENSIONS IN INCHES AND MILLIMETERS

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.

RCA linear integrated circuits

RF Amplifier CA3028

Monolithic Silicon

FEATURES

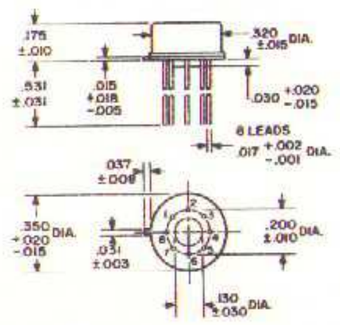
- Designed for use in Communications Equipment and Radio Receivers
- Balanced Differential Amplifier Configuration with Controlled Constant-Current Source to Provide Unexcelled Versatility
- Single-ended operation -- only one power supply required
- Operation from DC to 120 MHz

8-Pin TO-5

APPLICATIONS

- IF Amplifier (Differential or Cascode)
- Converter in the Commercial FM band
- Limiter
- Mixer
- Oscillator
- Companion Application Note, ICAN 5337 "Application of the RCA CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges". This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations.

DIMENSIONAL OUTLINE



Dimensions in Inches

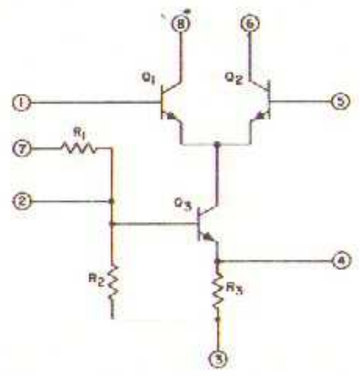


Fig. 1 - Schematic Diagram for CA3028.

ELECTRICAL CHARACTERISTICS T_A = 25° C

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028 Min.	Typ.	Max.	UNITS	TYPICAL CHARACTERISTICS CURVE Fig.
STATIC CHARACTERISTICS									
Quiescent Operating Current	I_6 or I_8	2a	V_{CC} = +9V	Differential-Amplifier	–	2.5	–	mA	2b
			V_{CC} = +12V		–	3.4	–		
Input Bias Current	I_I	3a	V_{CC} = +9V	Differential-Amplifier	–	29	77	μA	3b
			V_{CC} = +12V		–	44	106		
AGC Bias Current (Into Constant-Current Source Terminal No.7)	I_{AGC}	4a	V_{AGC} = +9V	–	–	1.28	–	mA	4b
			V_{AGC} = +12V		–	1.65	–		
Device Dissipation	P_T	5	V_{CC} = +9V	–	35	56	100	mW	–
			V_{CC} = +12V		–	113	–		
DYNAMIC CHARACTERISTICS									
Power Gain	G_P	6a	f = 100 MHz	Cascode	16	20	–	dB	6b
		7a, 7d	V_{CC} = +9V	Diff.-Ampl.	14	17	–		7b, 7e
		6a	f = 10.7 MHz	Cascode	35	39	–	dB	6b
		7a	V_{CC} = +9V	Diff.-Ampl.	28	32	–		7b
Noise Figure	NF	6a	f = 100 MHz	Cascode	–	7.2	9	dB	6c
		7a, 7d	V_{CC} = +9V	Diff.-Ampl.	–	6.7	9		7c, 7e
Input Admittance	Y_{11}	–	f = 10.7 MHz V_{CC} = +9V	Cascode	–	0.6 + j1.6	–	mmho	8
		–		Diff.-Ampl.	–	0.5 + j0.5	–		9
Reverse Transfer Admittance	Y_{12}	–		Cascode	–	0.0003 - j0	–	mmho	10
		–		Diff.-Ampl.	–	0.01 - j0.0002	–		11
Forward Transfer Admittance	Y_{21}	–		Cascode	–	99 - j18	–	mmho	12
		–		Diff.-Ampl.	–	-37 + j0.5	–		13
Output Admittance	Y_{22}	–		Cascode	–	0 + j0.08	–	mmho	14
		–		Diff.-Ampl.	–	0.04 + j0.23	–		15
Power Output (Untuned)	P_o	16a	f = 10.7 MHz V_{CC} = +9V	Diff.-Ampl. 50Ω Input-Output	–	5.7	–	mW	16b
Voltage Gain	A	17a	f = 10.7 MHz V_{CC} = +9V R_L = 1 KΩ	Cascode	–	98	–	–	17b
		17c		Diff.-Ampl.	–	32	–		17d
AGC Range (Max. Power Gain to Full Cutoff)	AGC	18a	f = 10.7 MHz V_{CC} = +9V	Diff.-Ampl.	–	62	–	dB	18b

RADIO CORPORATION OF AMERICA
ELECTRONIC COMPONENTS AND DEVICES, HARRISON, N.J.
Trademark(s) ® Registered
Marca(s) Registrada(s)
CA3028

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION ..... 300 mW

TEMPERATURE RANGE:

Operating ..... -55° C to +125° C

Storage ..... -65° C to +200° C

INPUT SIGNAL ..... 6 V p-p

Absolute-Maximum Voltage or Current Limits at T_A = 25° C:

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals.

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE (OR CURRENT) LIMITS NEGATIVE	POSITIVE	CONDITIONS TERMINAL	VOLTAGE
1	–	5 to 11	6, 7, 8 5 3	+12 +8 0
2	6	10	6, 7, 8 1, 5 3	+12 +8 0
3	6	12	6, 7, 8 1, 5	+12 +8
4	0 to 20 mA		6, 7, 8 1, 5 3	+12 +8 0
5	–	5 to 11	6, 7, 8 1 3	+12 +8 0
6	0	18	7, 8 1, 5 3	+12 +8 0
7	0	14	6, 8 1, 5 3	+12 +8 0
8	0	18	6, 7 1, 5 3	+12 +8 0

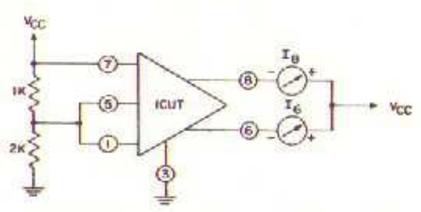


Fig. 2a - Quiescent Operating Current Test Circuit for CA3028.

DEFINITIONS OF TERMS

Input Bias Current

The average value (one-half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Quiescent Operating Current

The average (dc) value of the current in either output terminal.

AGC Bias Current

The current drawn by the device from the AGC-voltage source, at maximum AGC voltage.

Device Dissipation

The total power drain of the device with no signal applied and no external load current.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

TYPICAL CHARACTERISTIC

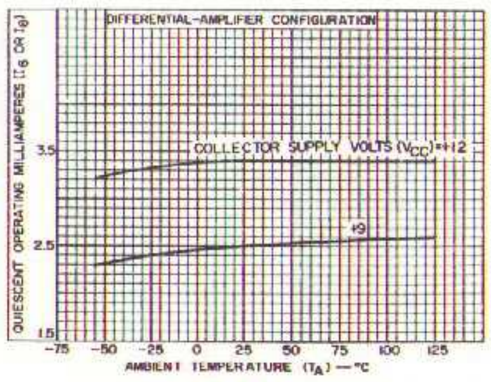


Fig. 2b - Quiescent Operating Current vs Ambient Temperature.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS

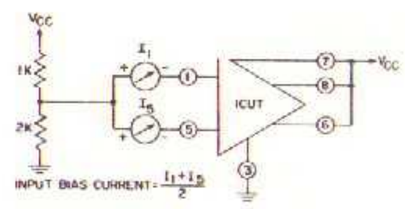


Fig. 3a - Input Bias Current Test Circuit.

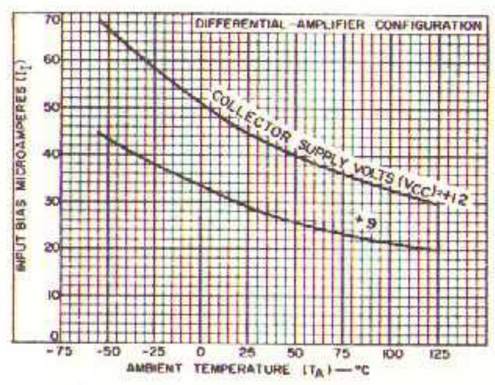


Fig. 3b - Input Bias Current vs Ambient Temperature.

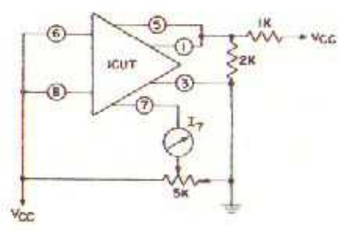


Fig. 4a - AGC Bias Current Test Circuit (Differential-Amplifier Configuration).

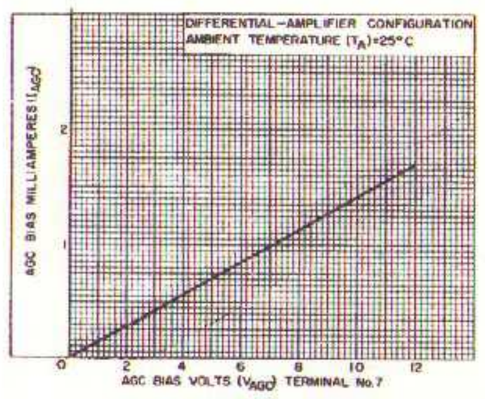


Fig. 4b - AGC Bias Current vs Bias Volts (Terminal No.7).

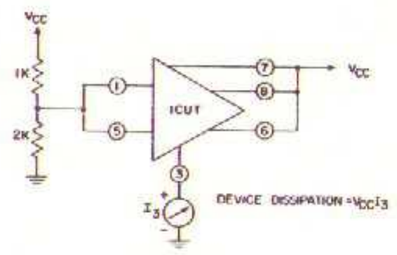
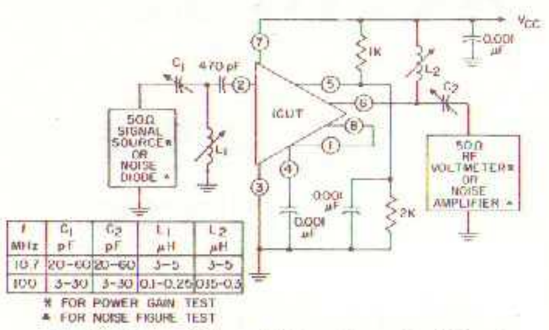


Fig. 5 - Device Dissipation Test Circuit.

TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS



f MHz	C_1 pF	C_2 pF	L_1 µH	L_2 µH
10.7	20-60	20-60	3-5	3-5
100	3-30	3-30	0.1-0.25	0.15-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.6a - Power Gain and Noise Figure Test Circuit (Cascode Configuration) for CA3028.

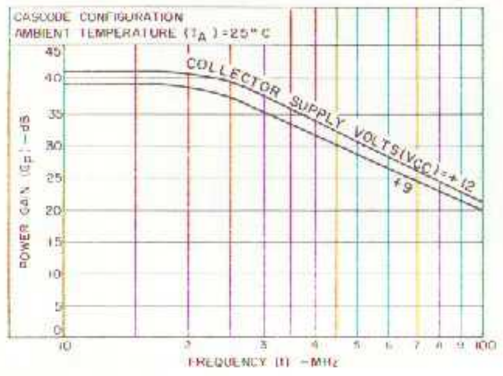


Fig.6b - Power Gain vs Frequency (Cascode Configuration).

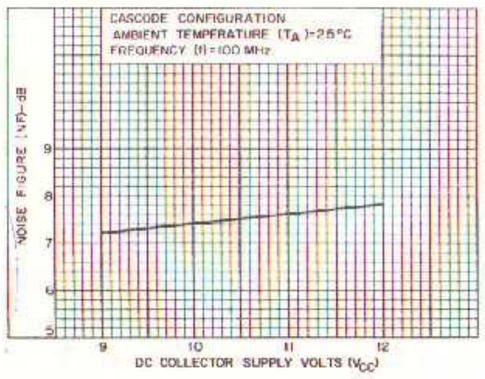
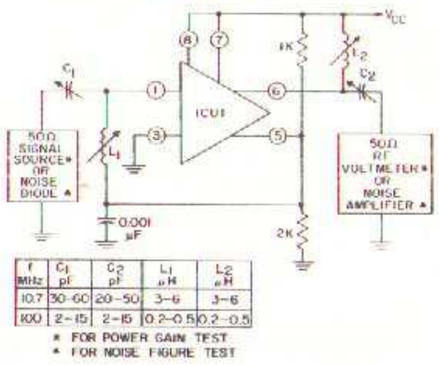


Fig.6c - 100 MHz Noise Figure vs Collector Supply Volts (Cascode Configuration).



f MHz	C_1 pF	C_2 pF	L_1 µH	L_2 µH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.7a - Power Gain and Noise Figure Test Circuit (Differential-Amplifier Configuration) for CA3028 (Terminal No.7 Connected to V_{CC}).

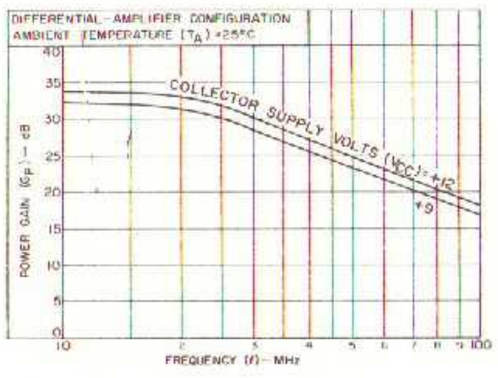


Fig.7b - Power Gain vs Frequency (Differential-Amplifier Configuration).

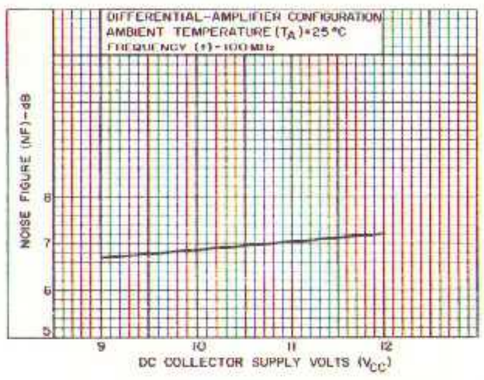


Fig.7c - 100 MHz Noise Figure vs Collector Supply Voltage (Differential-Amplifier Configuration).

TYPICAL ADMITTANCE PARAMETERS

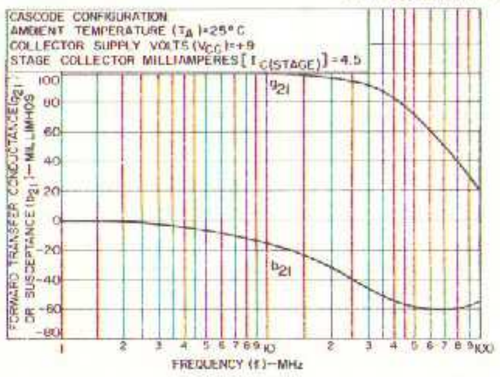


Fig.12 - Forward Transadmittance (Y_{21}) vs Frequency (Cascode Configuration).

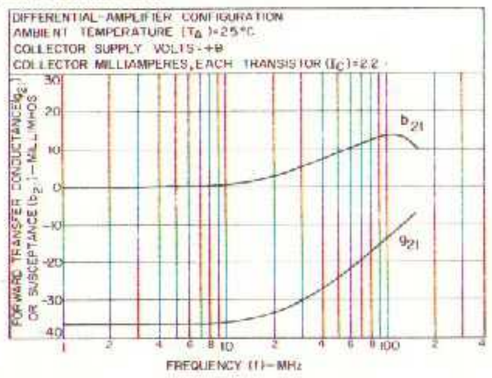


Fig.13 - Forward Transadmittance (Y_{21}) vs Frequency (Differential-Amplifier Configuration).

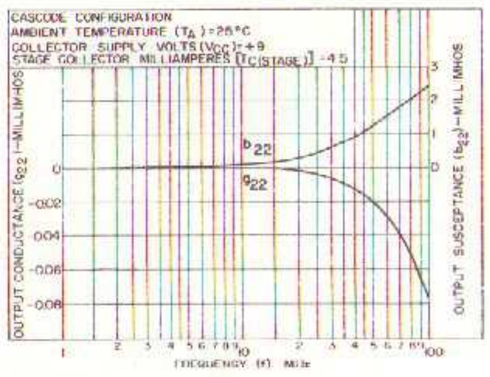


Fig.14 - Output Admittance (Y_{22}) vs Frequency (Cascade Configuration).

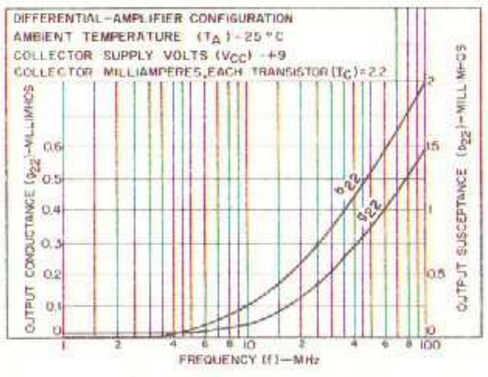


Fig.15 - Output Admittance (Y_{22}) vs Frequency (Differential-Amplifier Configuration).

TYPICAL POWER OUTPUT TEST CIRCUIT AND CHARACTERISTIC

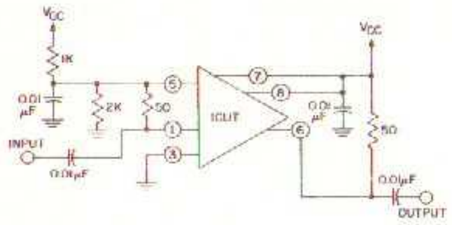


Fig.16a - Output Power Test Circuit for CA3028.

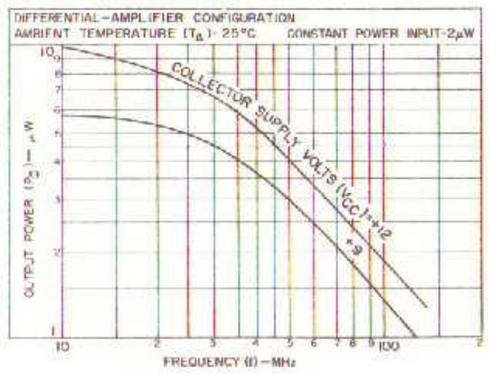
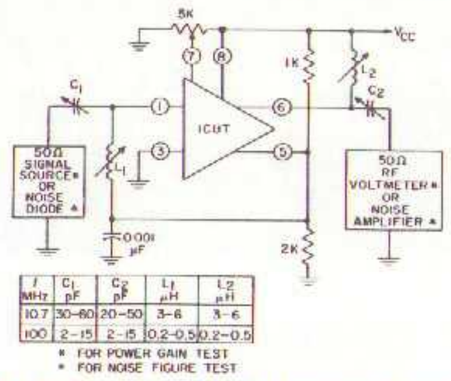


Fig.16b - Output Power vs Frequency 50Ω Input and 50Ω Output (Differential-Amplifier Configuration).

TEST CIRCUIT AND TYPICAL CHARACTERISTICS



f MHz	C_1 pF	C_2 pF	L_1 µH	L_2 µH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
* FOR NOISE FIGURE TEST

Fig.7d - Power Gain and Noise Figure Test Circuit (Differential-Amplifier Configuration).

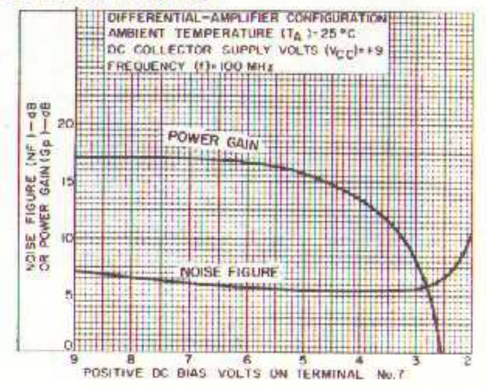


Fig.7e - 100 MHz Noise Figure and Power Gain vs Base-to-Emitter Bias (Terminal No.7).

TYPICAL ADMITTANCE PARAMETERS

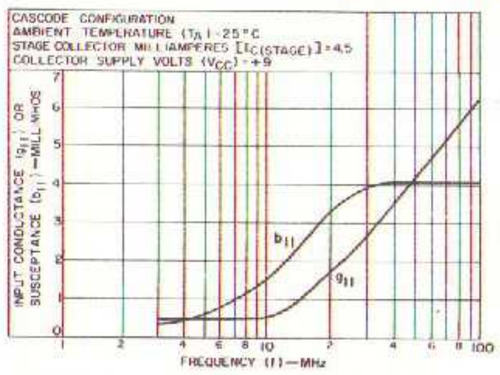


Fig.8 - Input Admittance (Y_{11}) vs Frequency (Cascade Configuration).

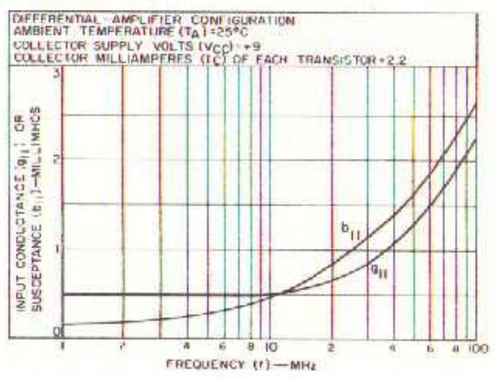


Fig.9 - Input Admittance (Y_{11}) vs Frequency (Differential-Amplifier Configuration).

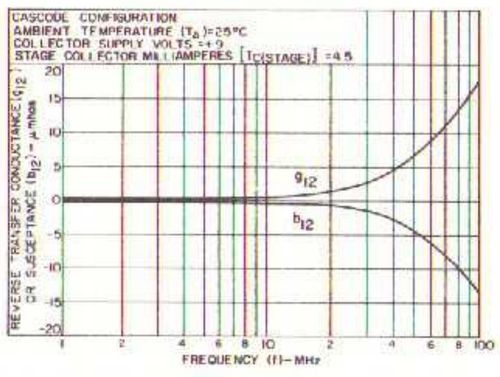


Fig.10 - Reverse Transadmittance (Y_{12}) vs Frequency (Cascade Configuration).

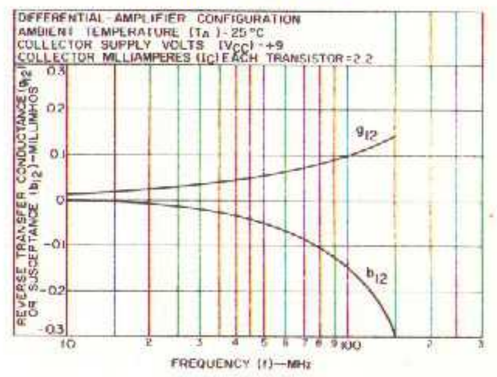


Fig.11 - Reverse Transadmittance (Y_{12}) vs Frequency (Differential-Amplifier Configuration).

TEST CIRCUITS AND TYPICAL CHARACTERISTICS

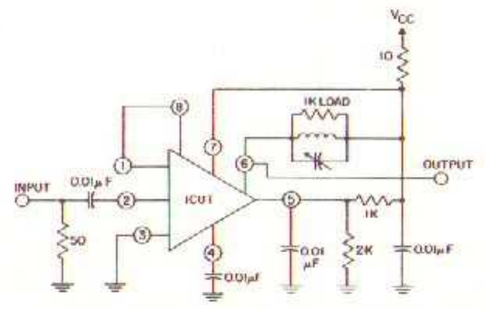


Fig.17a - Transfer Characteristic (Voltage Gain) Test Circuit (10.7 MHz) Cascode Configuration.

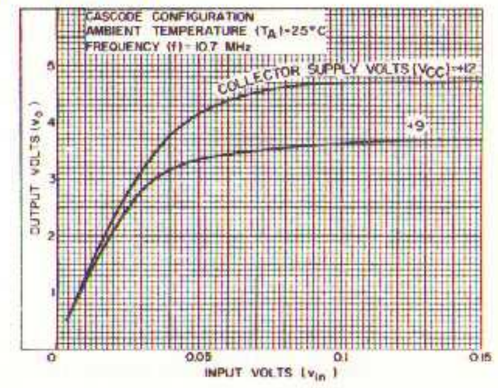


Fig.17b - Transfer Characteristics (Cascade Configuration).

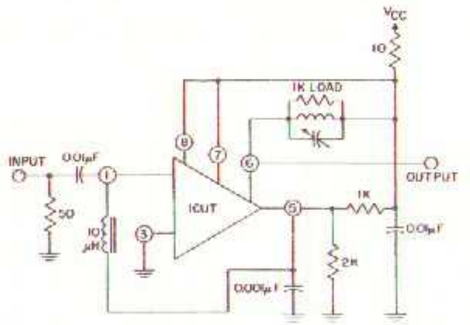


Fig.17c - Transfer Characteristic (Voltage Gain) Test Circuit (10.7 MHz) Differential-Amplifier Configuration.

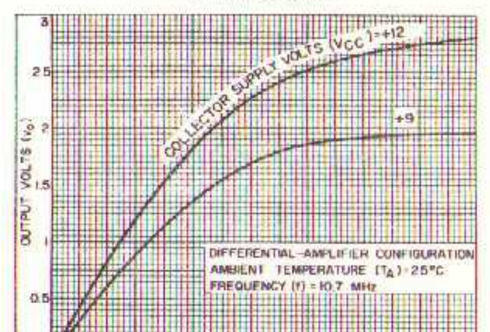
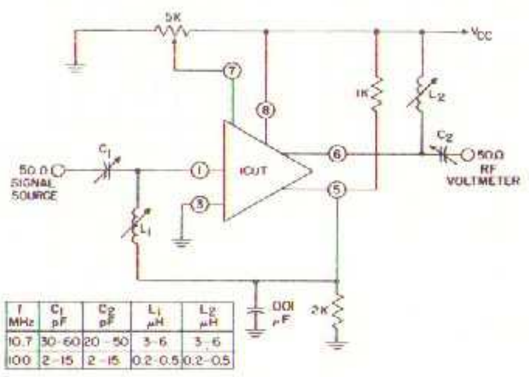


Fig.17d - Transfer Characteristics (Differential-Amplifier Configuration).



f MHz	C_1 pF	C_2 pF	L_1 µH	L_2 µH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

Fig.18a - AGC Range Test Circuit (Differential Amplifier).

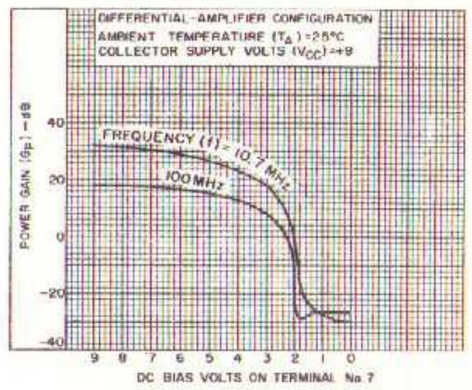


Fig.18b - AGC Characteristics.

MOTOROLA Semiconductors
BOX 955 • PHOENIX, ARIZONA 85001

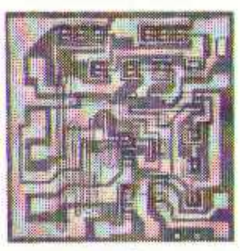
MC1430
MC1431

OPERATIONAL AMPLIFIER INTEGRATED CIRCUITS

- MONOLITHIC
- SILICON EPITAXIAL PASSIVATED

JUNE 1967 — DS 9057R1
(REPLACES DS 9057)

MONOLITHIC OPERATIONAL AMPLIFIER



. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High Open Loop Gain
  A_{VOL} = 74 dB typical
- Large Output Voltage Swing
  typically ± 5 V @ ± 6 V Supply
- Low Output Impedance
  Z_{out} = 25 ohms typical
- High Slew Rate
  typically 4.5 V/μs

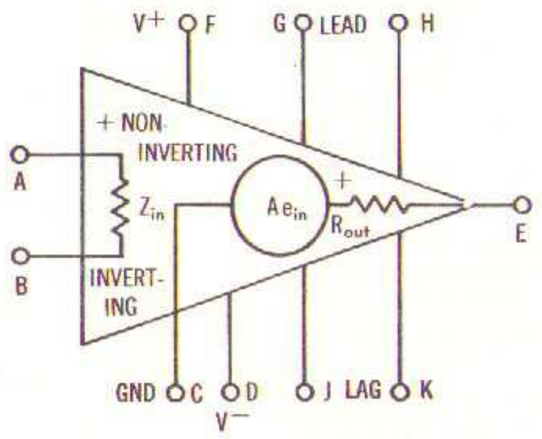
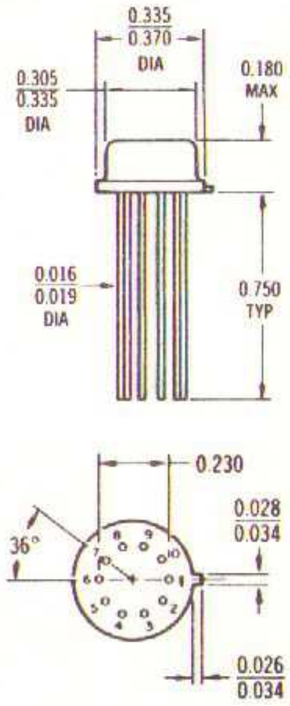


FIGURE 1 – EQUIVALENT CIRCUIT BOTH TYPES

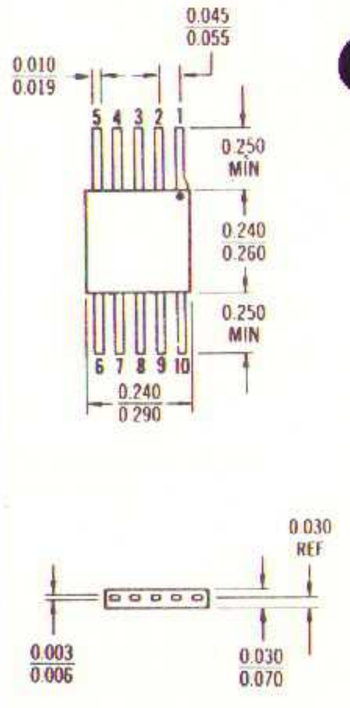
TO-91

CASE 71
10-PIN METAL CAN
G SUFFIX



Pin 4 connected to case

CASE 72
10-PIN FLAT PACKAGE
F SUFFIX



Lead 1 identified by color dot or by shoulder on pin.

All leads electrically isolated from package.

PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	J	K
"F" & "G" Pkgs.	1	2	3	4	5	6	7	8	9	10
"P" Package	4	6	8	7	11	12	13	14	1	2

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+8	Vdc
Power Supply Voltage	V^-	-8	Vdc
Differential Input Signal	V_{in}	±5	Volts
Load Current	I_L	10	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above 25°C		4.6	mW/°C
Flat Package		500	mW
Derate above 25°C		3.3	mW/°C
Plastic Package		400	mW
Derate above 25°C		3.3	mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}		°C
Metal Can and Flat Package		-55 to +150	
Plastic Package		-55 to +125	

*For full temperature range (-55°C to +125°C) see MC1530-MC1531 data sheet.

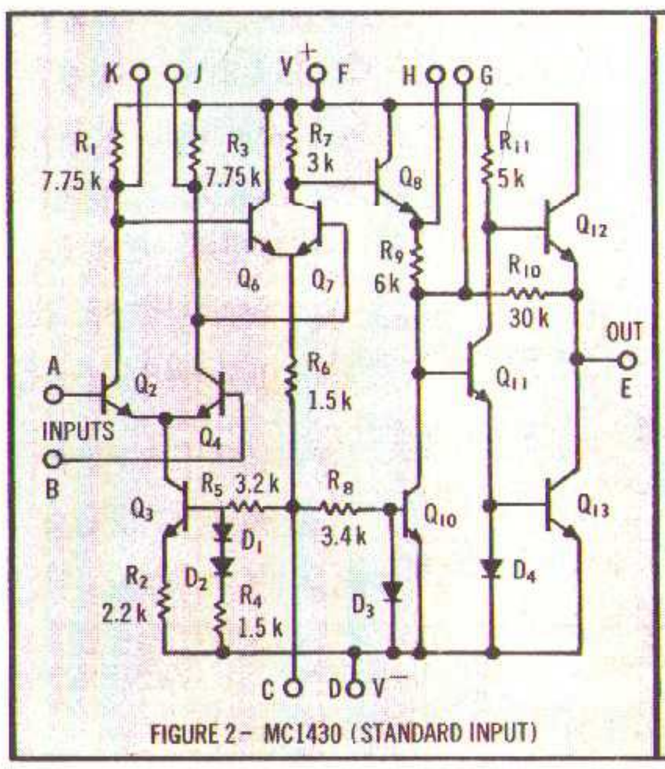


FIGURE 2 – MC1430 (STANDARD INPUT)

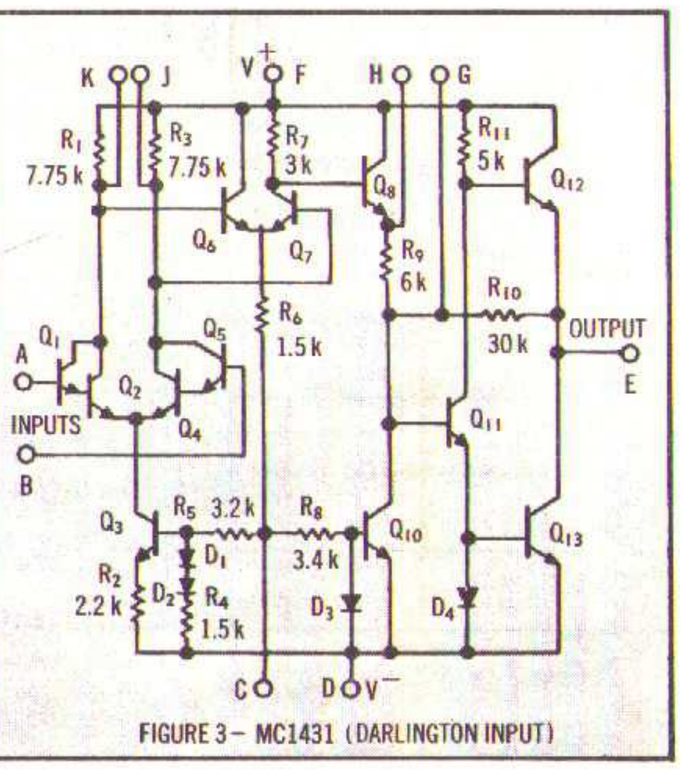
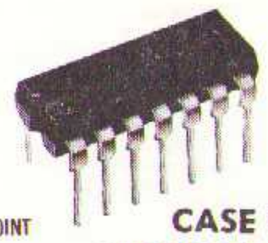
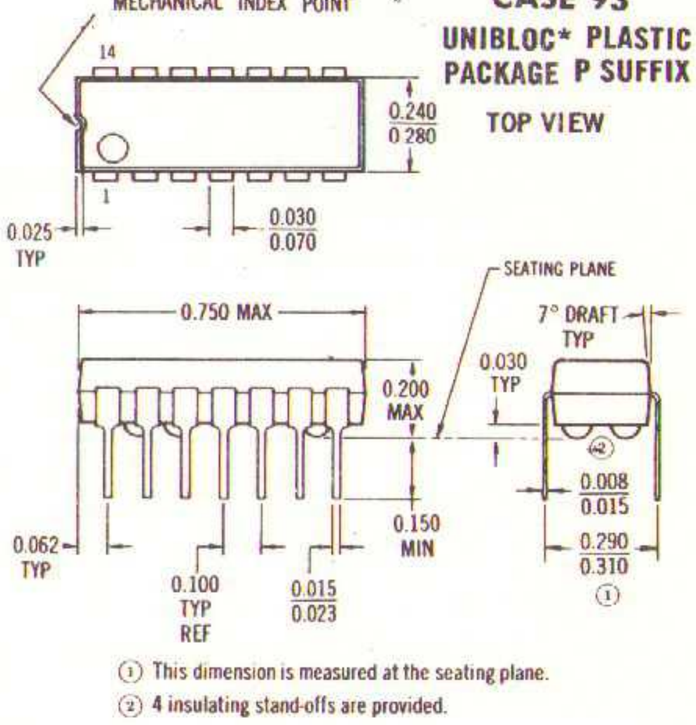


FIGURE 3 – MC1431 (DARLINGTON INPUT)

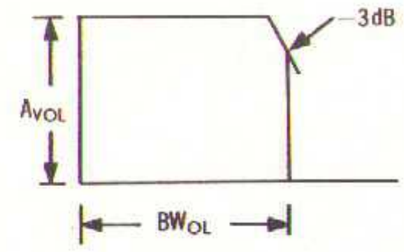
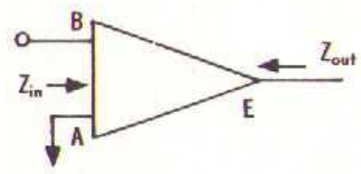
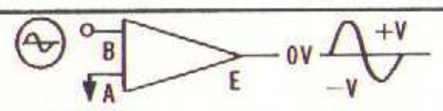
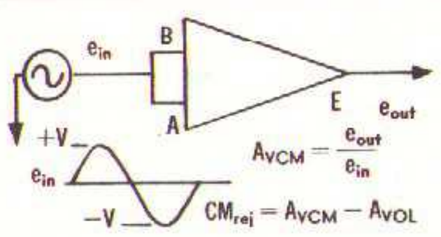
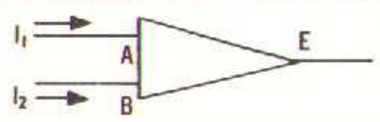
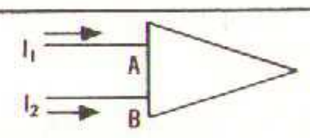
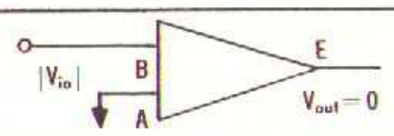


CASE 93
UNIBLOC* PLASTIC
PACKAGE P SUFFIX



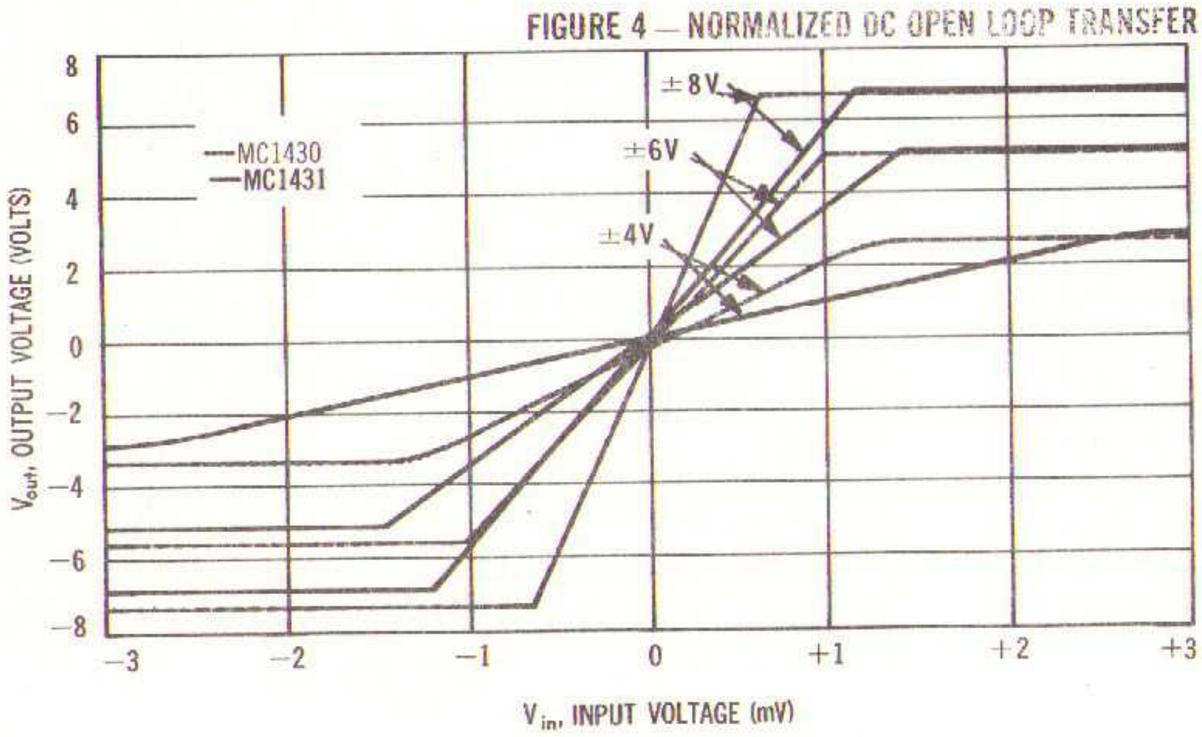
① This dimension is measured at the seating plane.
② 4 insulating stand-offs are provided.

ELECTRICAL CHARACTERISTICS ($V^+ = +6$ Vdc, $V^- = -6$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions*	Characteristic		Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain	MC1430	A_{VOL}	69	74	—	dB
		MC1431		62	71	—	dB
		MC1430		3000	5000	—	V/V
		MC1431		1500	3500	—	V/V
	Open Loop Bandwidth (no roll-off capacitance)	MC1430	BW_{OL}	1.0	1.2	—	MHz
		MC1431		0.15	0.4	—	
	Output Impedance (f = 20 Hz)	MC1430, MC1431	Z_{out}	—	25	50	ohms
	Input Impedance (f = 20 Hz)	MC1430	Z_{in}	5k	15k	—	ohms
		MC1431		300k	600k	—	
	Output Voltage Swing (1000 ohm Load)	MC1430, MC1431	V_{out}	±4.0	±5.0	—	V_{peak}
	Input Common Mode Voltage Swing	MC1430	CMV_{in}	±2.0	±2.5	—	V_{peak}
		MC1431		±2.0	±2.2	—	
	Common Mode Rejection Ratio	MC1430	CM_{rej}	65	75	—	dB
		MC1431		60	75	—	
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$	MC1430	I_b	—	5	15	μA
		MC1431		—	0.1	0.3	
	Input Offset Current $I_{io} = I_1 - I_2$	MC1430	I_{io}	—	0.4	4	μA
		MC1431		—	0.01	0.1	
	Input Offset Voltage	MC1430	$\|V_{io}\|$	—	2	10	mV
		MC1431		—	5	15	
	DC Power Dissipation (Power Supply = ±6 V, V_{out} = 0)		P_D	—	110	150	mW
	Input Offset Voltage		$\|V_{io}\|$				mV
	+75°C	MC1430		—	3.0	12.0	
	0°C			—	3.0	11.0	
	+75°C	MC1431		—	6.0	18.0	
	0°C			—	6.0	16.5	

*All definitions imply linear operation (V_{io} = 0)

FIGURE 4 — NORMALIZED DC OPEN LOOP TRANSFER CHARACTERISTICS



RECOMMENDED OPERATING CONDITIONS

1. For High Slew Rate use Circuit A, Figure 9
2. For Minimum Noise use Circuit B, Figure 9
3. For operational stability Power Supply decoupling should be employed at all times.
4. Self Biasing network used to hold output voltage less than ±1 volt dc (quiescent)

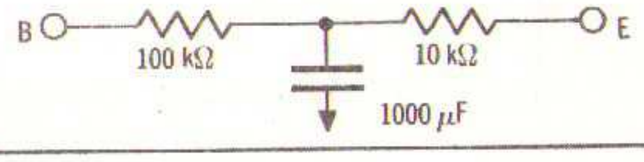
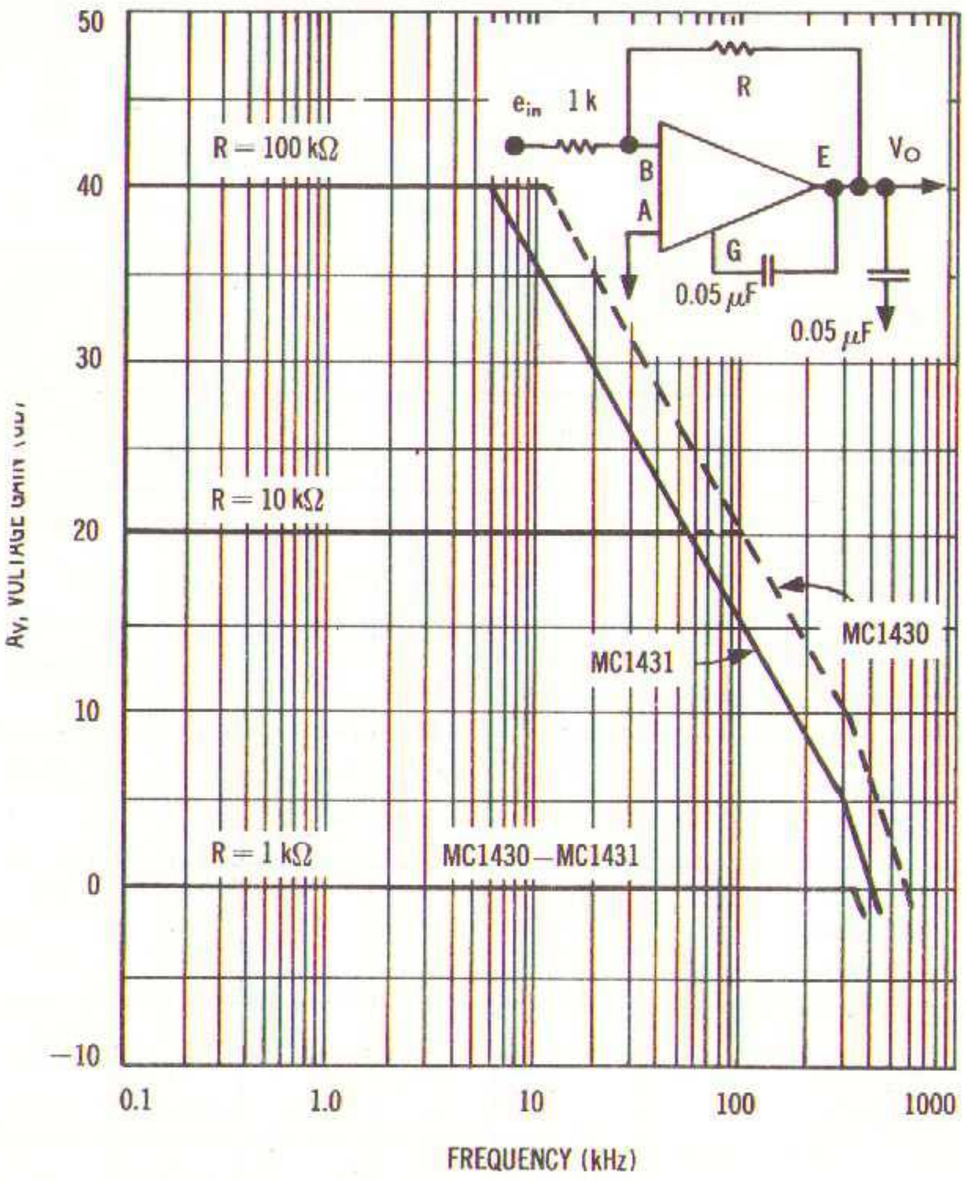


FIGURE 5 — VOLTAGE GAIN versus FREQUENCY
(Rolloff Applied To Output Amplifier)



(Rolloff Applied To Input Differential Amplifier)

FIGURE 6 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY
(Rolloff Applied To Input Differential Amplifier)

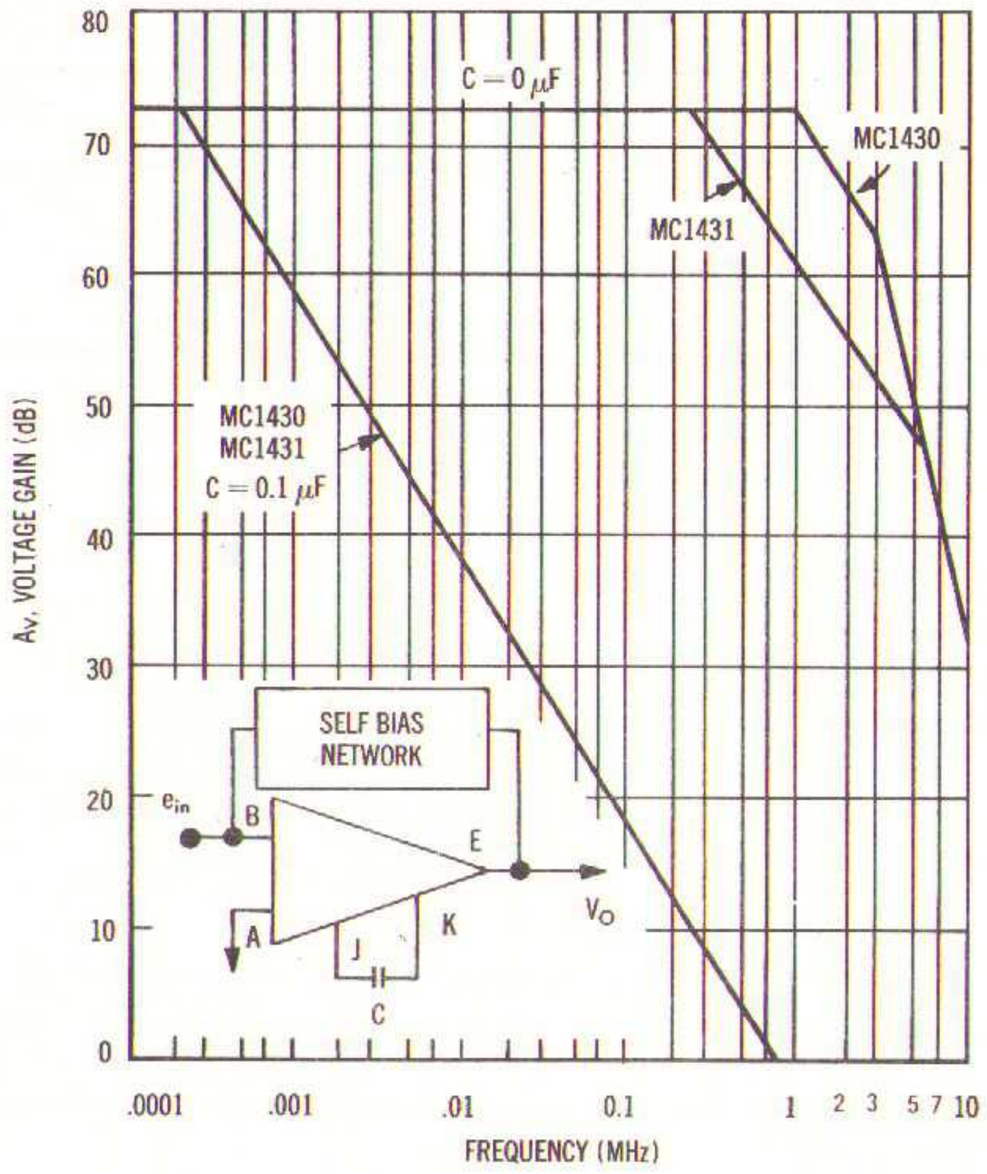


FIGURE 7 — VOLTAGE GAIN versus MINIMUM ROLLOFF CAPACITANCE

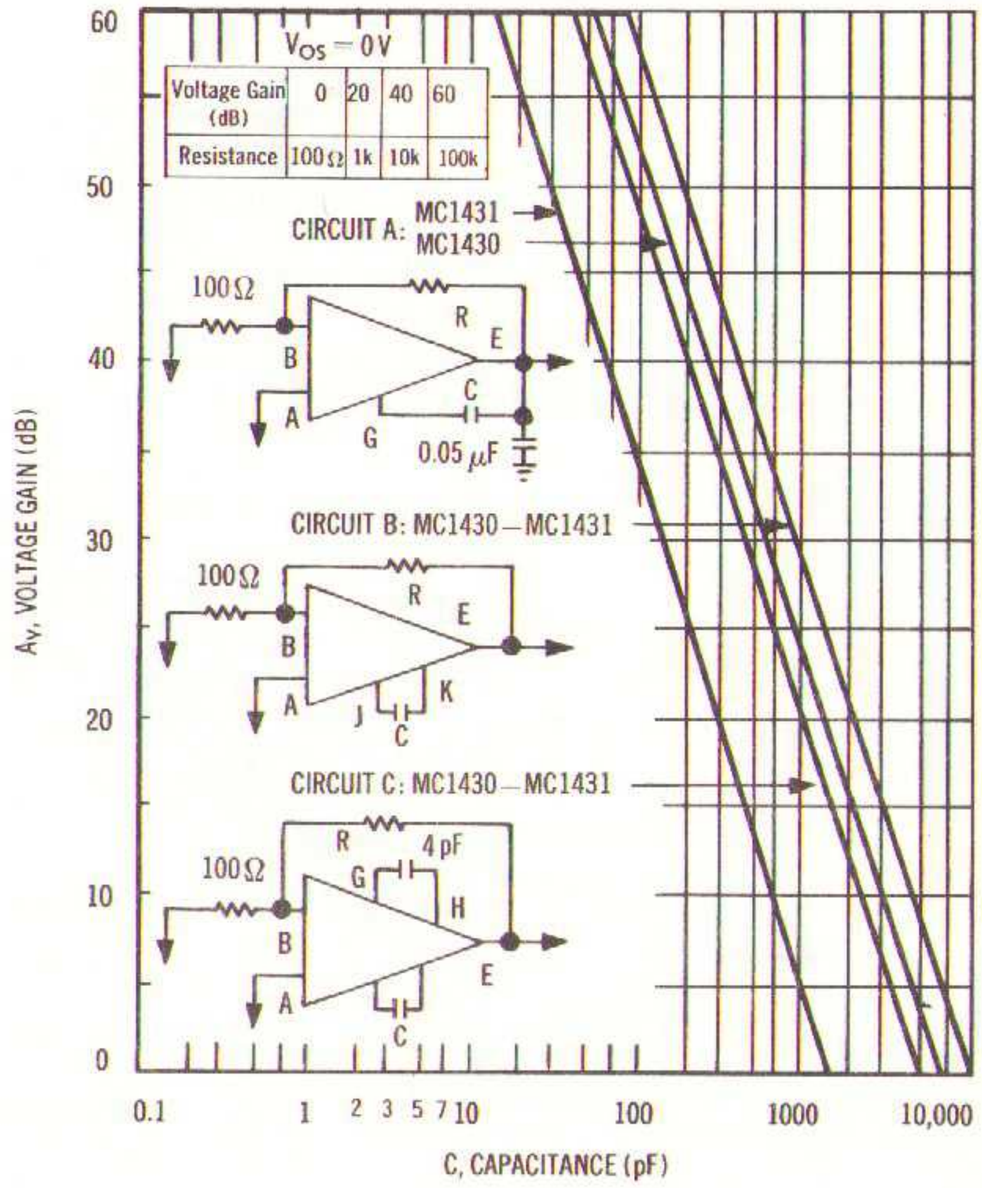
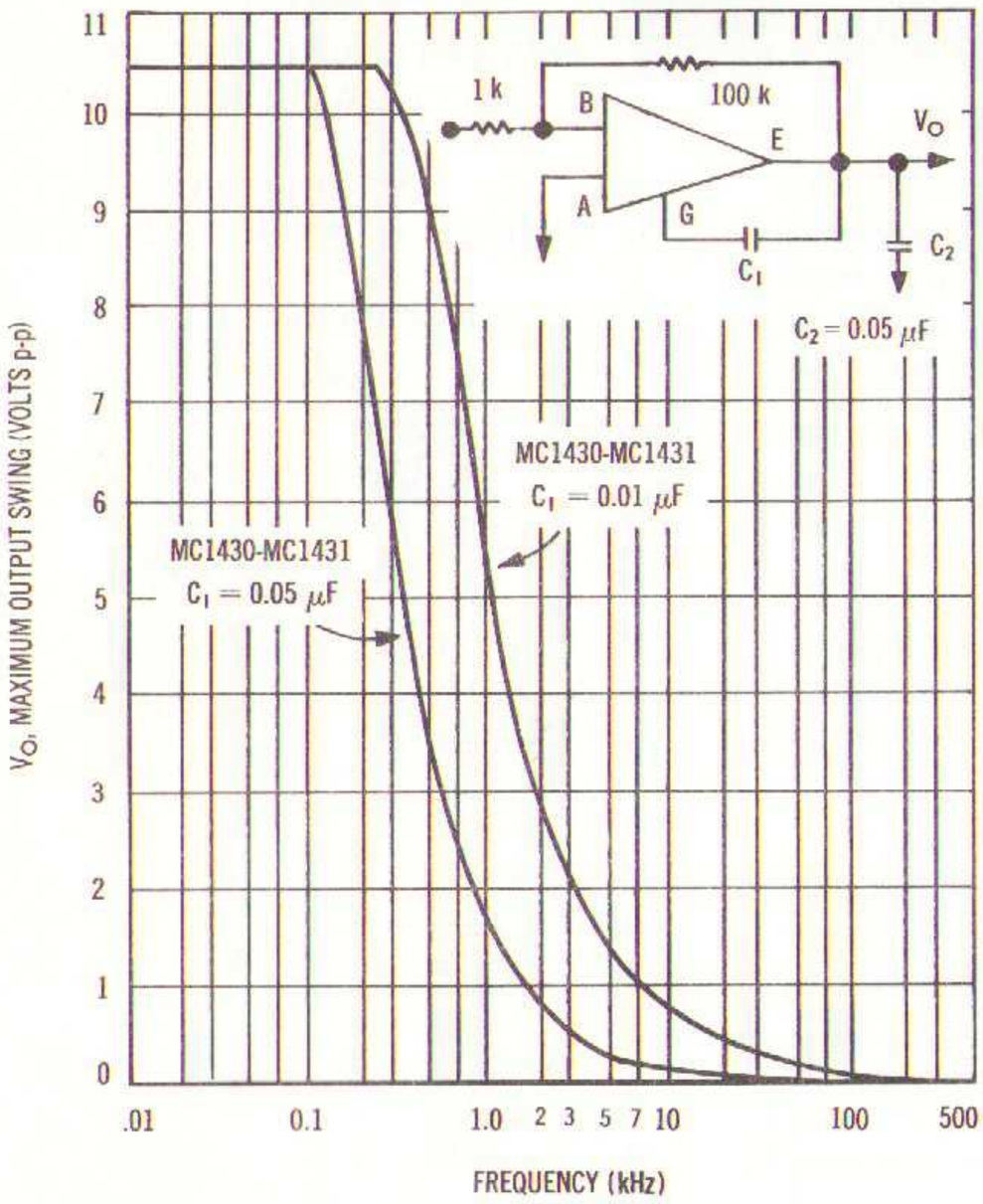


FIGURE 8 — MAXIMUM OUTPUT VOLTAGE SWING versus FREQUENCY

(Rolloff Applied To Output Amplifier)



(Rolloff Applied To Input Differential Amplifier)

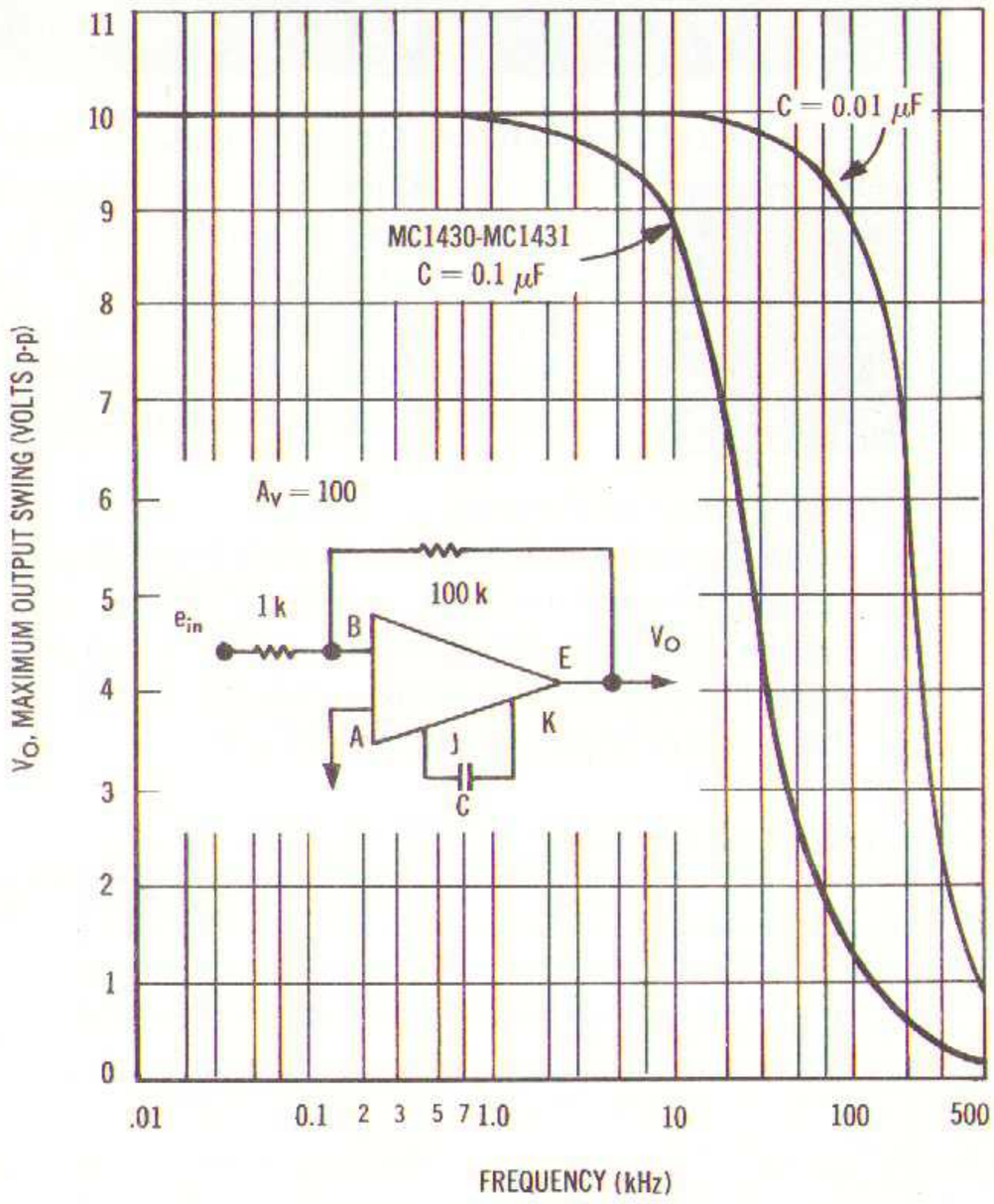


FIGURE 9 — SLEW RATE versus ROLLOFF CAPACITANCE

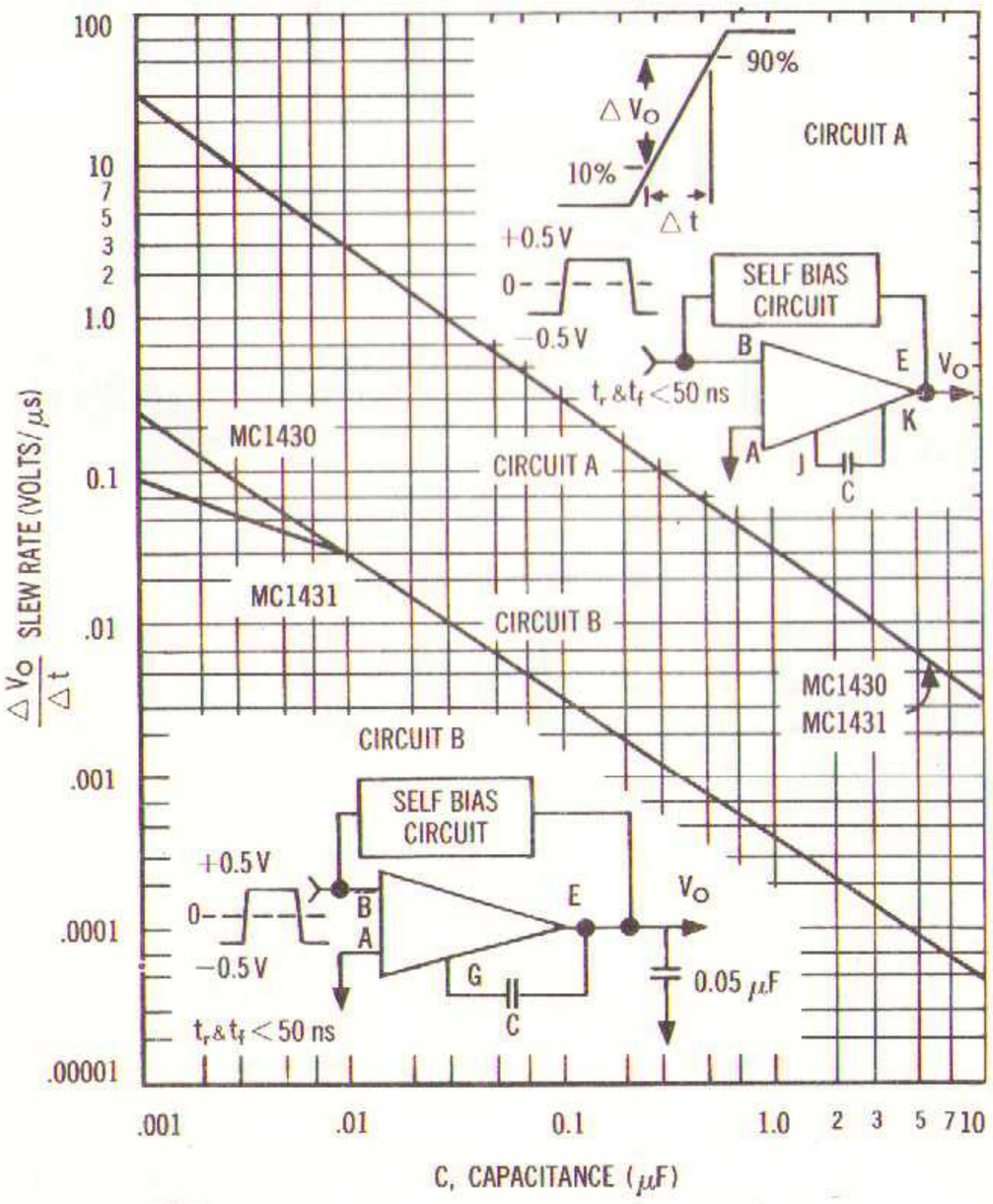
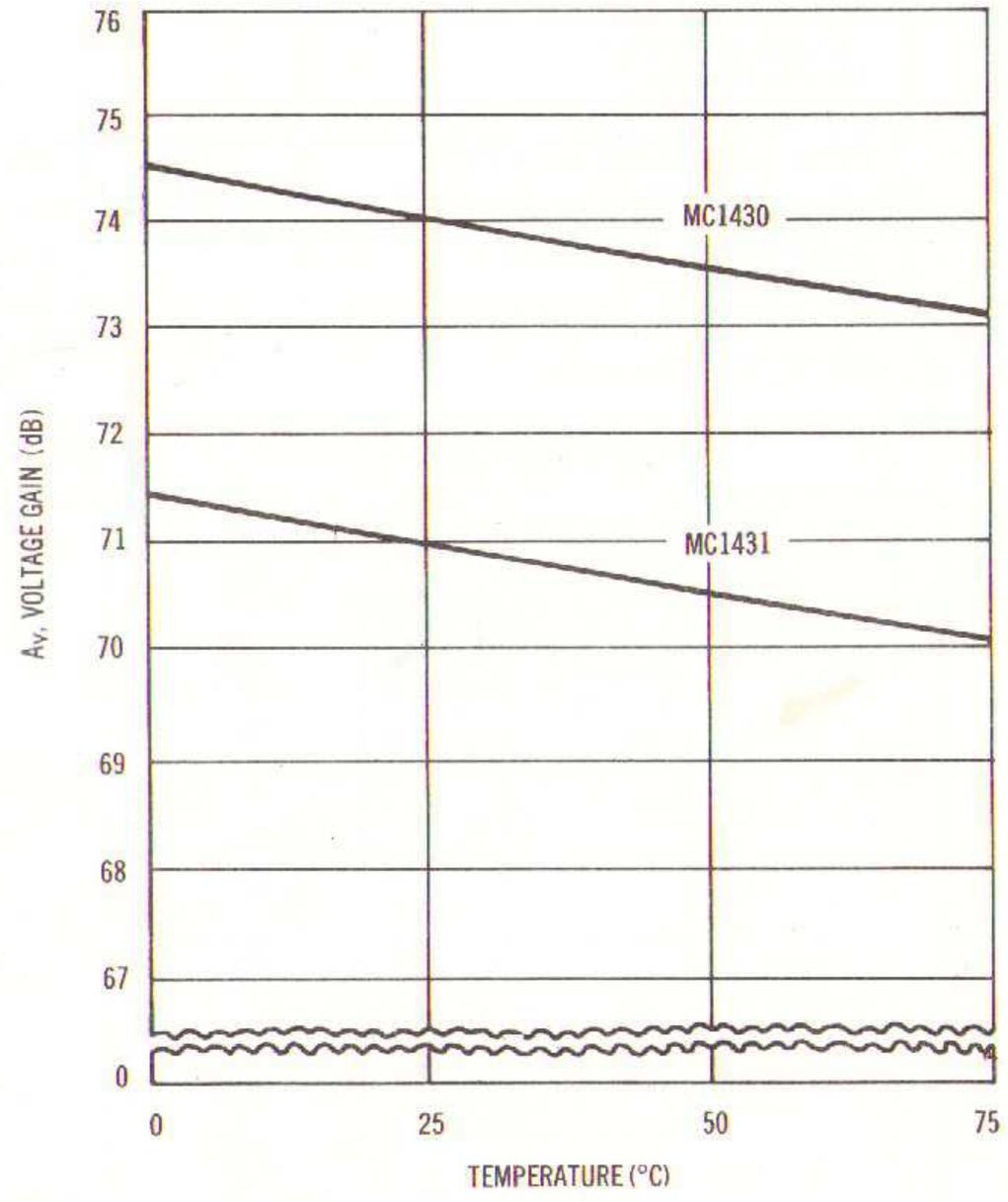


FIGURE 10 — OPEN LOOP VOLTAGE GAIN



MOTOROLA Semiconductor Products Inc.

MOTOROLA Semiconductors

BOX 955 • PHOENIX, ARIZONA 85001

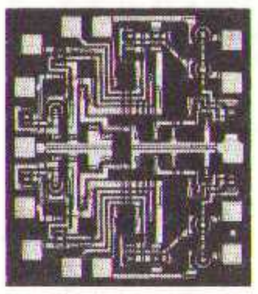
MC1435

DUAL OPERATIONAL AMPLIFIERS INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

AUGUST 1967 – DS 9085

MONOLITHIC DUAL OPERATIONAL AMPLIFIERS



. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

Typical Amplifier Features:

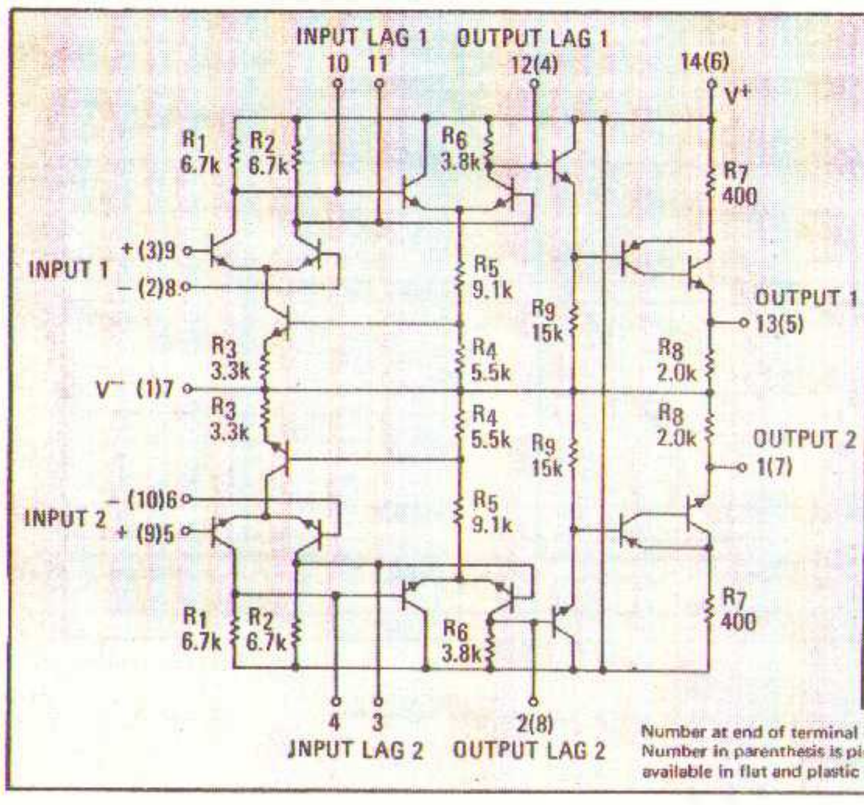
- High Open Loop Gain Characteristics – A_{VOL} = 7,000
- Low Temperature Drift – ±10 μV/°C
- Large Output Voltage Swing – ±3.6 V typ @ ±6.0 V supply
- Low Input Offset Voltage – 1.0 mV
- Low Input Noise Voltage – 0.5 μV

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+9.0 -9.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	+5.0 -4.0	Volts
Output Short Circuit Duration	I_S	Continuous	
Power Dissipation (package limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C Plastic Package Derate above 25°C	P_D	 680 4.6 500 3.3 400 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range Metal Can and Flat Package Plastic Package	T_{stg}	 -65 to +150 -65 to +125	°C

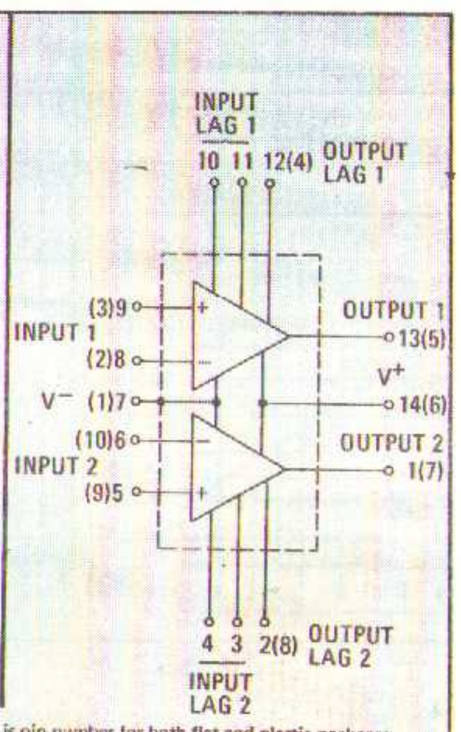
*For full temperature range (-55°C to +125°C) and characteristic curves, see MC1535 data sheet.

CIRCUIT SCHEMATIC

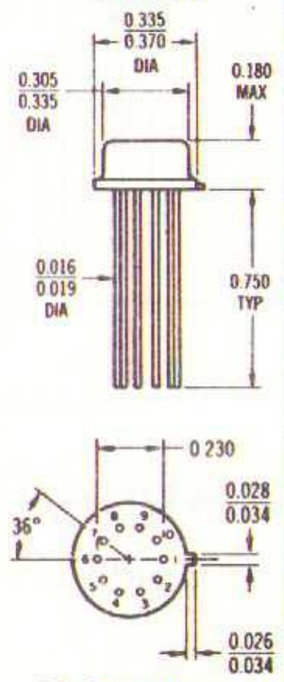


Number at end of terminal is pin number for both flat and plastic packages. Number in parenthesis is pin number for metal can package. Input lag available in flat and plastic packages.

EQUIVALENT CIRCUIT

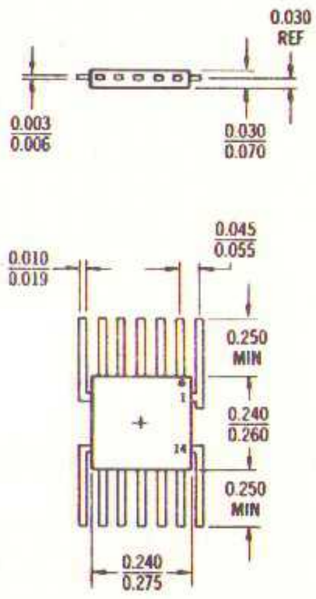


10-PIN METAL CAN G SUFFIX (CASE 71)



Pin 7 connected to case

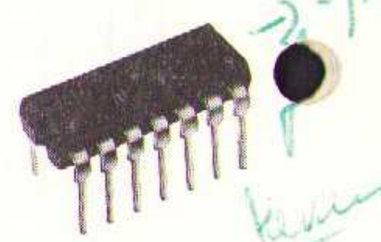
14-PIN FLAT PACKAGE F SUFFIX CASE 83 (TO-86)

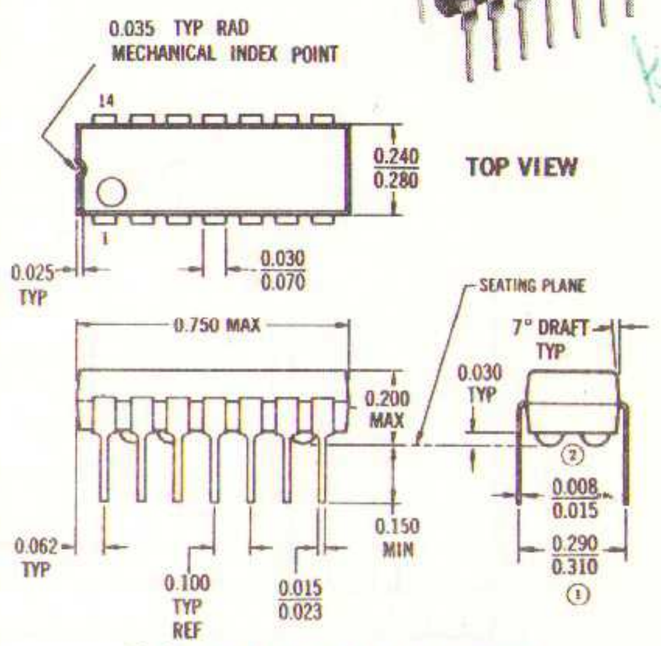


Lead 1 identified by color dot or elbow

All leads electrically isolated from package.

UNIBLOC* PLASTIC PACKAGE P SUFFIX (CASE 93)





① This dimension is measured at the seating plane.

② 4 insulating stand-offs are provided.

Pin 7 is connected to substrate and is at V^- potential

*Trademark of Motorola Inc.

MOTOROLA Semiconductor Products Inc.

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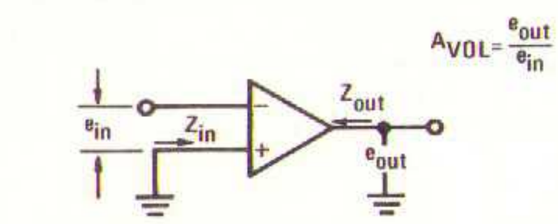
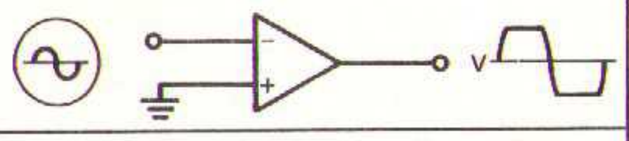
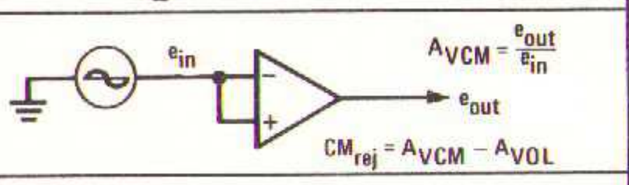
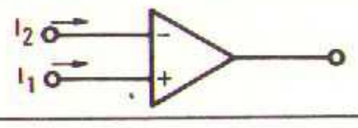
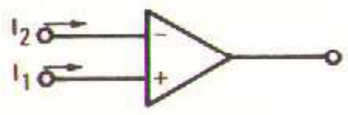
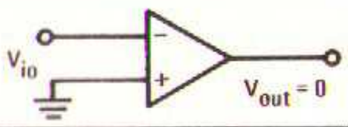
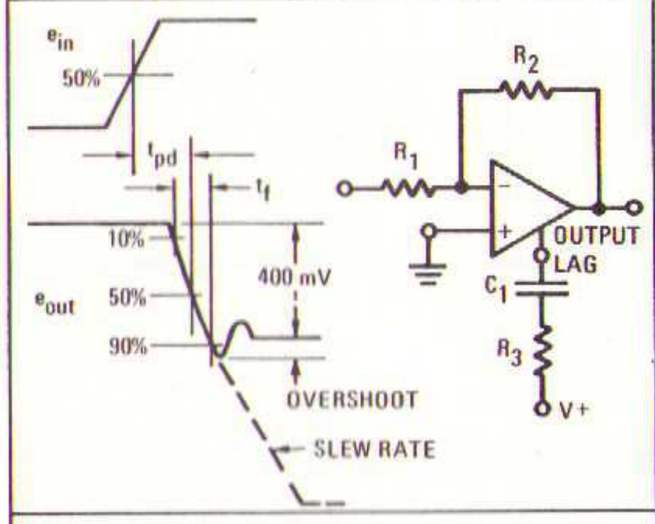
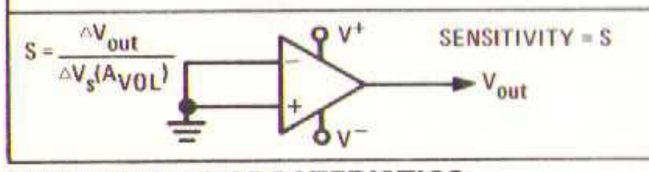
ELECTRICAL CHARACTERISTICS (Each Amplifier) (V^+ = +6.0Vdc, V^- = –6.0Vdc, T_A = 25°C unless otherwise noted)

Characteristic Definitions (linear) operations	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (T_A = 0°C to +75°C)	A_{VOL}	3,500 71	7,000 77	- -	V/V dB
	Output Impedance (f = 20 Hz)	Z_{out}	-	1.7	-	kΩ
	Input Impedance (f = 20 Hz)	Z_{in}	10	45	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ)	V_{out}	5.0	7.0	-	V_{p-p}
	Input Common Mode Voltage Swing	CMV_{in}	+3.0 -2.0	+3.9 -2.7	- -	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	60	90	-	dB
	Input Bias Current $\left(I_b=\frac{I_1+I_2}{2}\right)$, ($T_A$ = +25°C) (T_A = 0°C)	I_b	- -	1.2 3.6	5.0 10	μA
	Input Offset Current ($I_{io}=I_1-I_2$) ($I_{io}=I_1-I_2$, T_A = 0°C) ($I_{io}=I_1-I_2$, T_A = +75°C)	I_{io}	- - -	0.05 - -	0.5 1.5 1.5	μA
	Input Offset Voltage (T_A = 25°C) R_S = 50Ω (T_A = 0°C to + 75°C)	V_{io}	- -	1.0 -	5.0 7.5	mV
	Step Response {Gain = 100, 30% overshoot, R_1 = 4.7 kΩ, R_2 = 470 kΩ, R_3 = 150 Ω, C_1 = 1,000 pF}	t_f t_{pd} dV_{out}/dt ①	- - -	0.8 0.1 7.0	- - -	μs μs V/μs
	{Gain = 10, 10% overshoot, R_1 = 47 kΩ, R_2 = 470 kΩ, R_3 = 47 Ω, C_1 = 0.01 μF}	t_f t_{pd} dV_{out}/dt ①	- - -	0.4 0.3 4.0	- - -	μs μs V/μs
	{Gain = 1, 5% overshoot, R_1 = 47 kΩ, R_2 = 47 kΩ, R_3 = 4.7 Ω, C_1 = 0.1 μF}	t_f t_{pd} dV_{out}/dt ①	- - -	0.5 0.25 0.67	- - -	μs μs V/μs
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = 0°C to +75°C)	TC_{Vio}	-	3.0	-	μV/°C
	Average Temperature Coefficient of Input Offset Current (T_A = 0°C to +75°C)	TC_{Iio}		2.0		nA/°C
	DC Power Dissipation (Power Supply = ± 6.0 V, V_{out} = 0)	P_D	-	100	180	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	50	-	μV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	100	-	μV/V

MATCHING CHARACTERISTICS

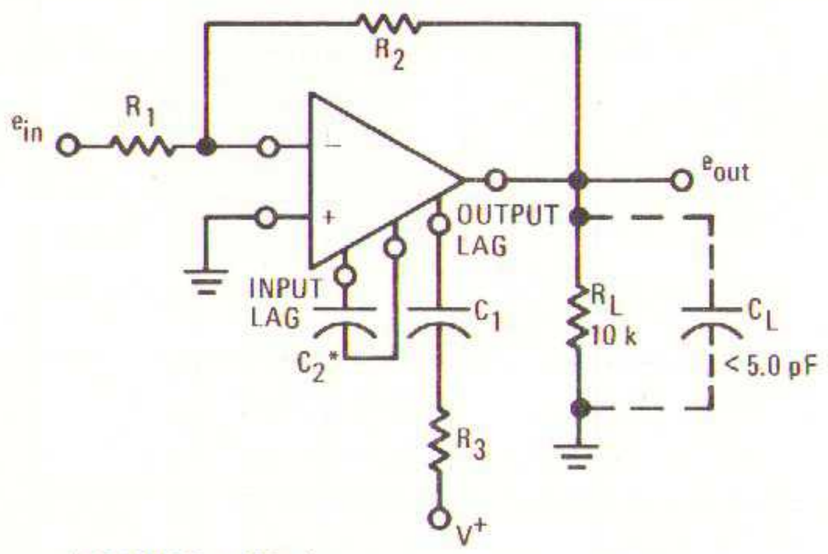
Same characteristic definitions as shown for each amplifier above.	Open Loop Voltage Gain	$A_{VOL1}-A_{VOL2}$	-	±1.0	-	dB
	Input Bias Current	$I_{b1}-I_{b2}$	-	±0.15	-	μA
	Input Offset Current	$I_{io1}-I_{io2}$	-	±0.02	-	μA
	Average Temperature Coefficient	$TC_{Iio1}-TC_{Iio2}$		±0.1		nA/°C
	Input Offset Voltage	$V_{io1}-V_{io2}$	-	±0.1	-	mV
	Average Temperature Coefficient	$TC_{Vio1}-TC_{Io2}$		±0.5		μV/°C
	Channel Separation (See Fig. 10) (f = 10 kHz)	$\frac{e_{out\ 1}}{e_{out\ 2}}$	-	-60	-	dB

① dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

$V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, $T_A = 25°C$

FIGURE 1 – TEST CIRCUIT



*MC1435 F and P only.

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS $R_1(\Omega)$	$R_2(\Omega)$	C_1(pF)	$R_3(\Omega)$	C_2(pF)	OUTPUT NOISE (mV rms)
2	1	100	4.7 k	470 k	1,000	150	0	1.7
	1A	or 100	4.7 k	470 k	0	∞	510	2.1
	2	10	47 k	470 k	10,000	47	0	1.0
	2A	or 10	47 k	470 k	0	∞	5,000	2.1
	3	1	47 k	47 k	100,000	4.7	0	0.12
	3A	or 1	47 k	47 k	0	∞	50,000	0.46
3	1	100	4.7 k	470 k	1,000	150	0	1.7
		or 100	4.7 k	470 k	0	∞	510	2.1
	2	10	47 k	470 k	10,000	47	0	1.0
		or 10	47 k	470 k	0	∞	5,000	2.1
	3	1	47 k	47 k	100,000	4.7	0	0.12
		or 1	47 k	47 k	0	∞	50,000	0.46
4	1	AVOL	100	∞	1,000	150	0	8.1
		or AVOL	100	∞	0	∞	510	8.1
	2	AVOL	100	∞	10,000	47	0	5.5
		or AVOL	100	∞	0	∞	5,000	5.5
	3	AVOL	100	∞	100,000	4.7	0	4.4
		or AVOL	100	∞	0	∞	50,000	4.4

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY

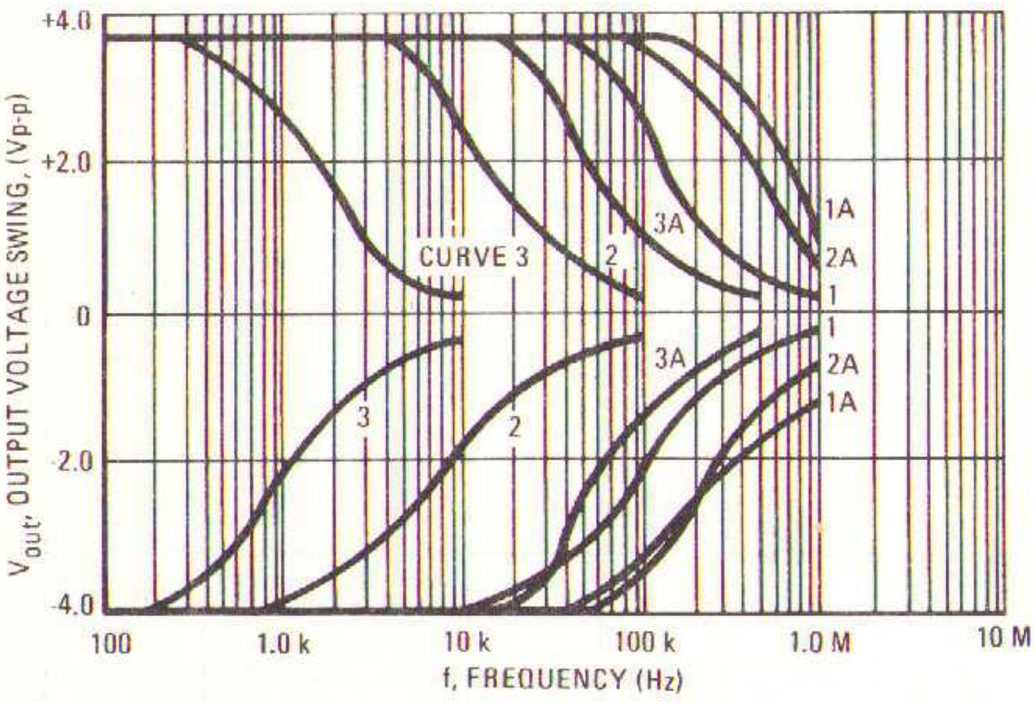


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

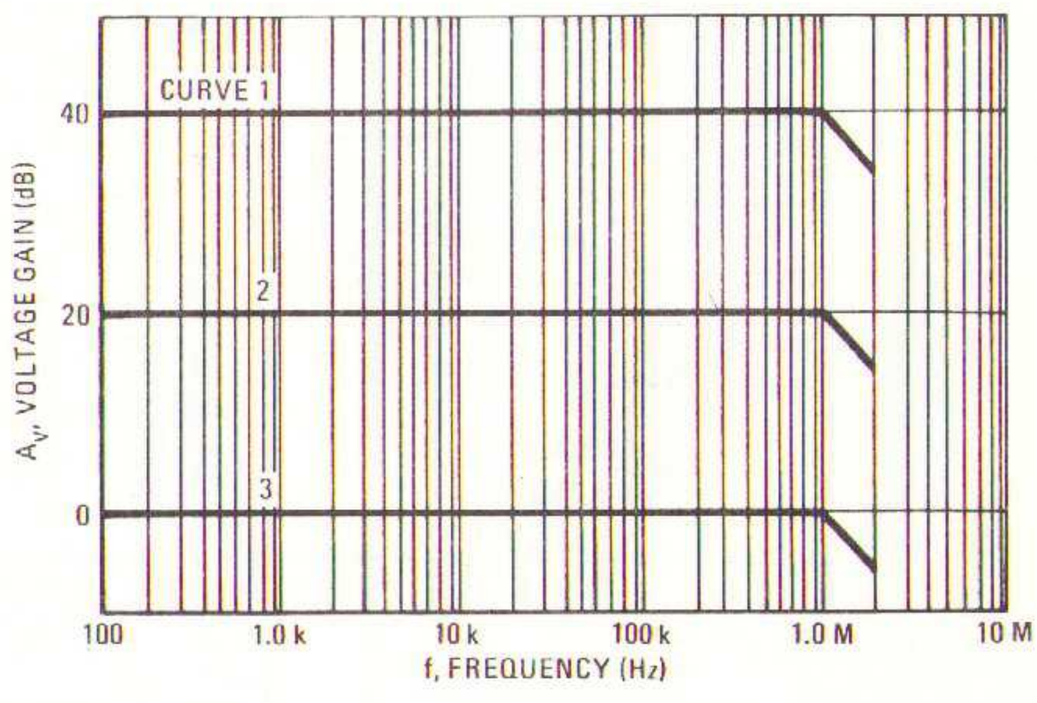


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

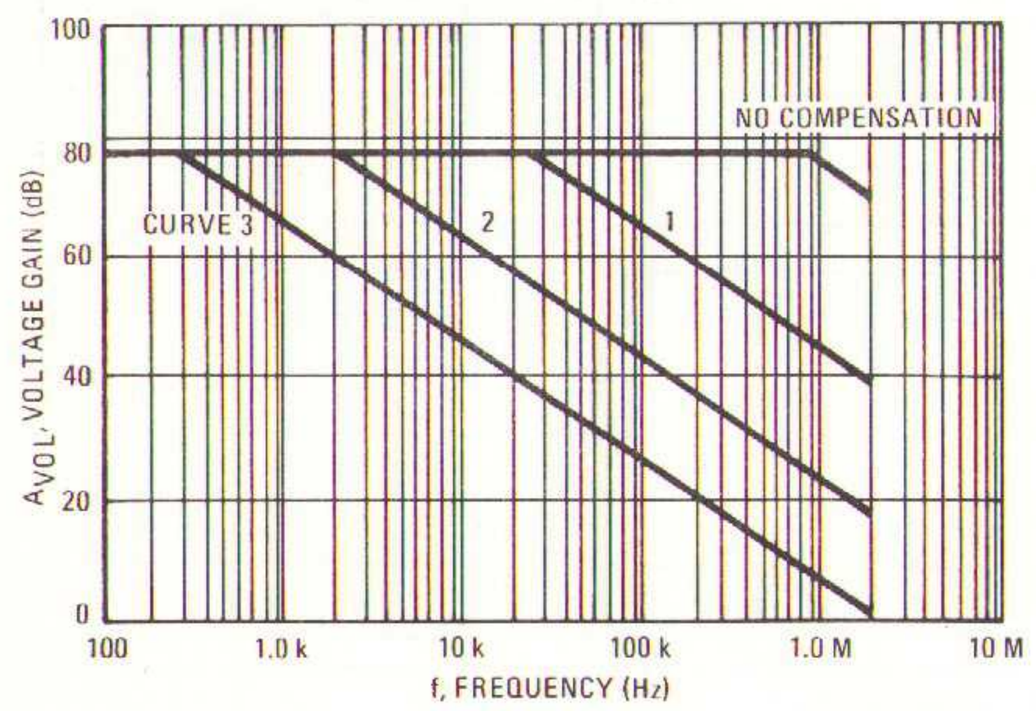


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE

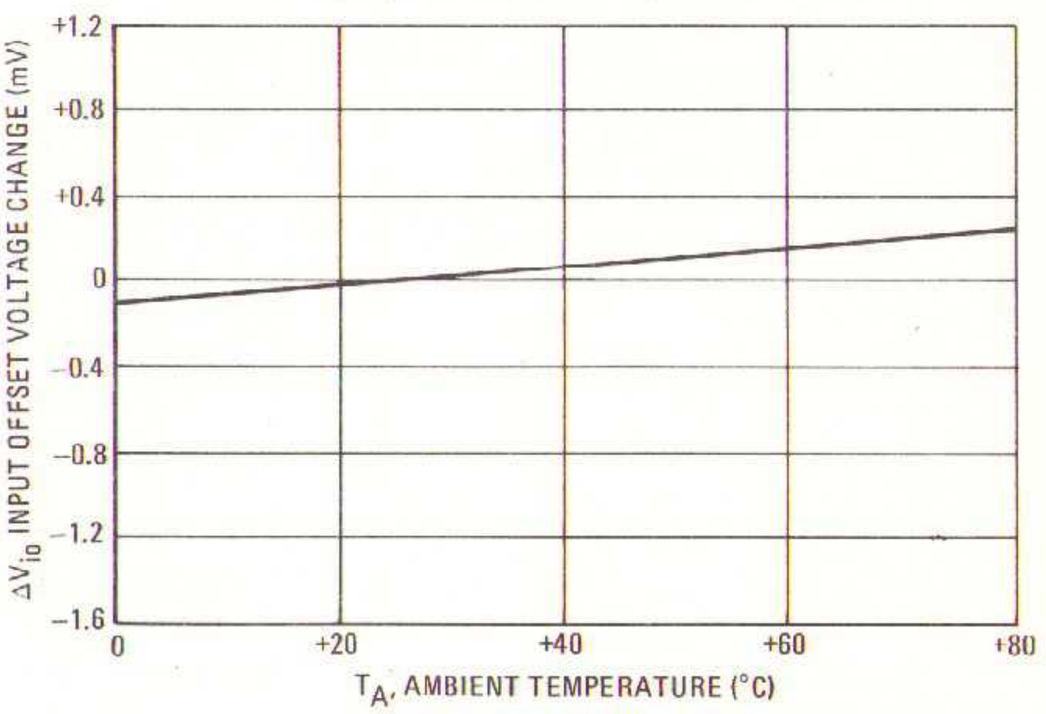


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

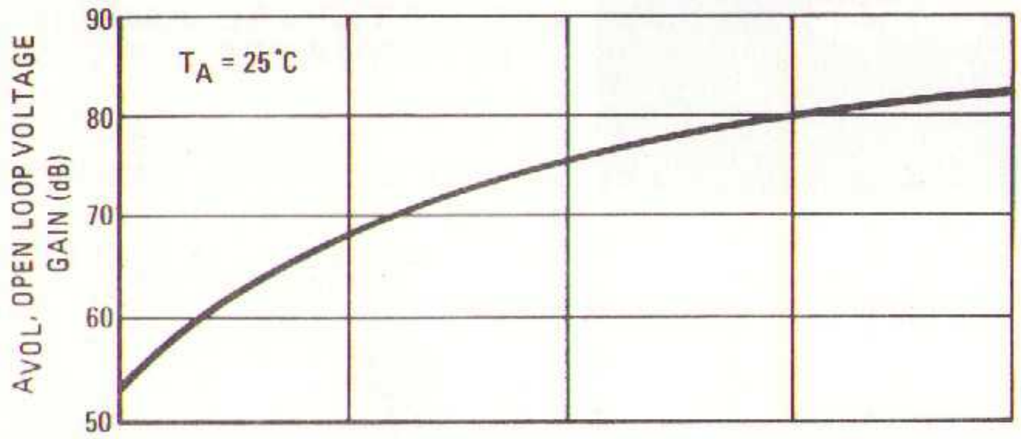


FIGURE 1 – COMMON MODE SWING versus POWER SUPPLY VOLTAGE

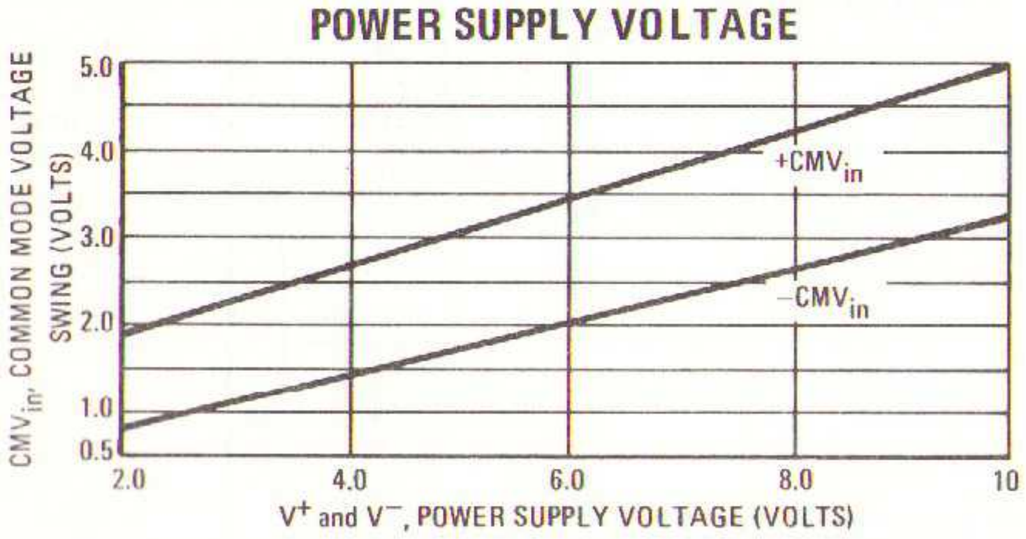


FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

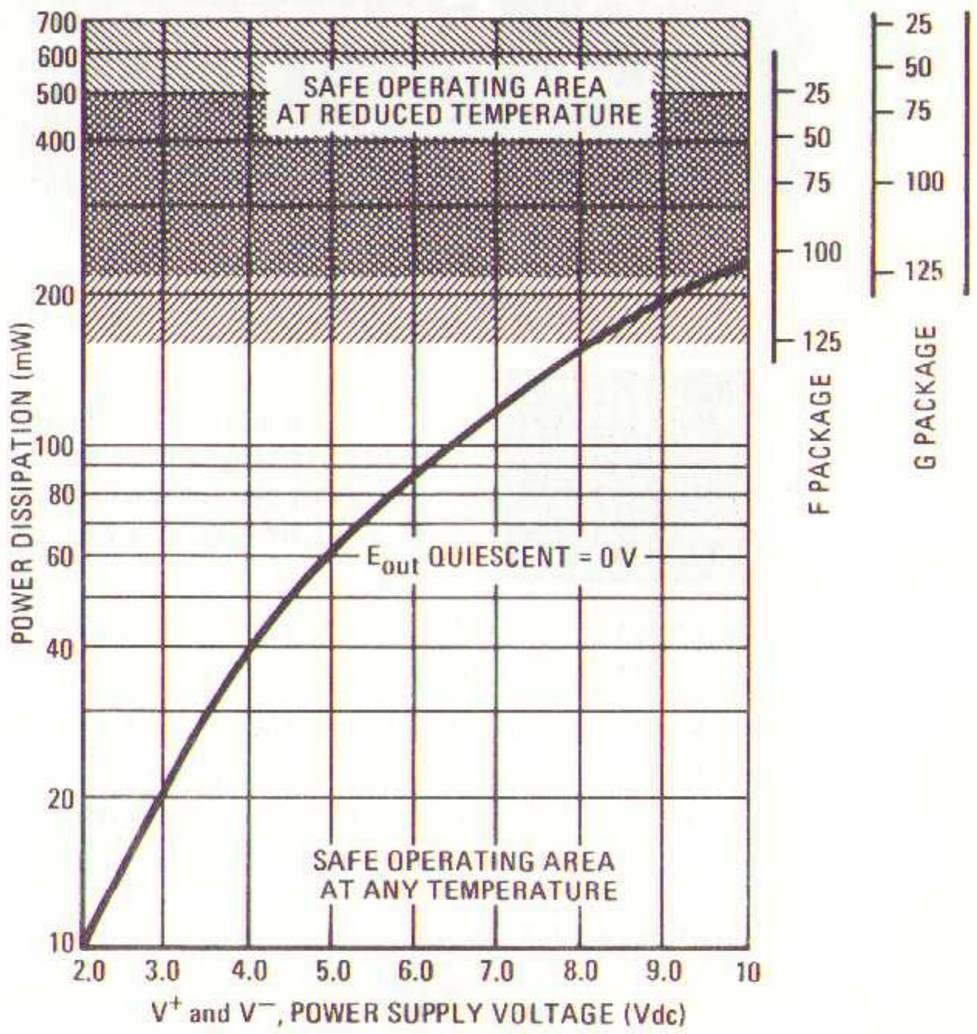
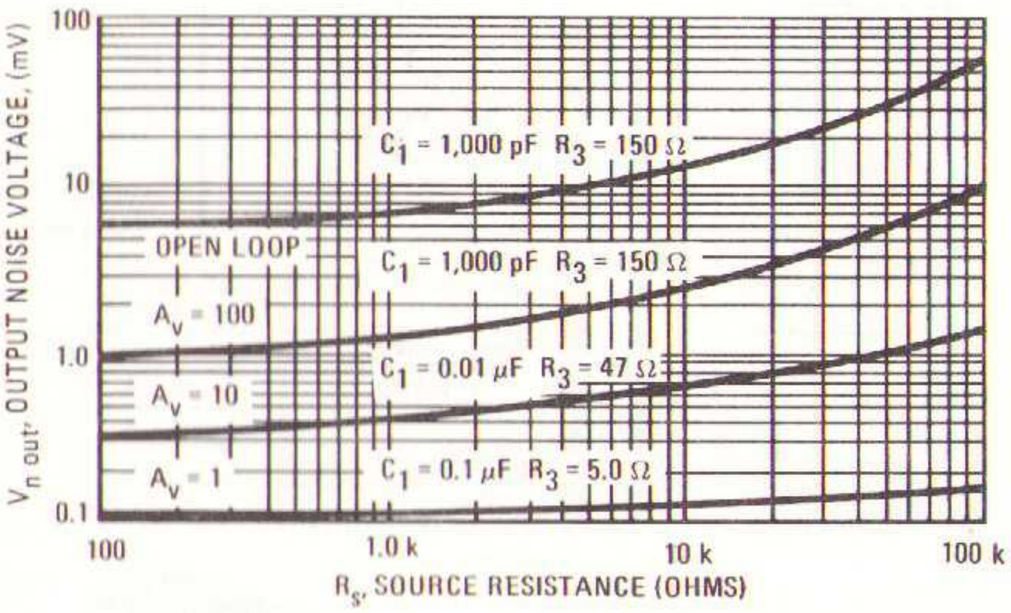


FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE



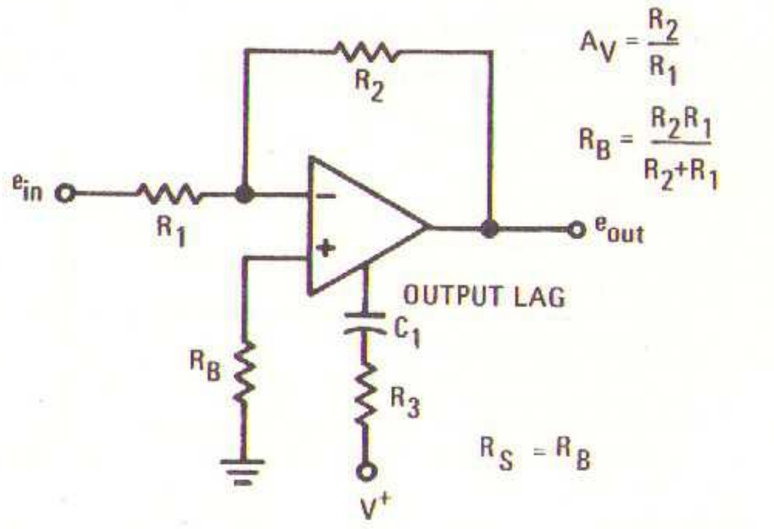
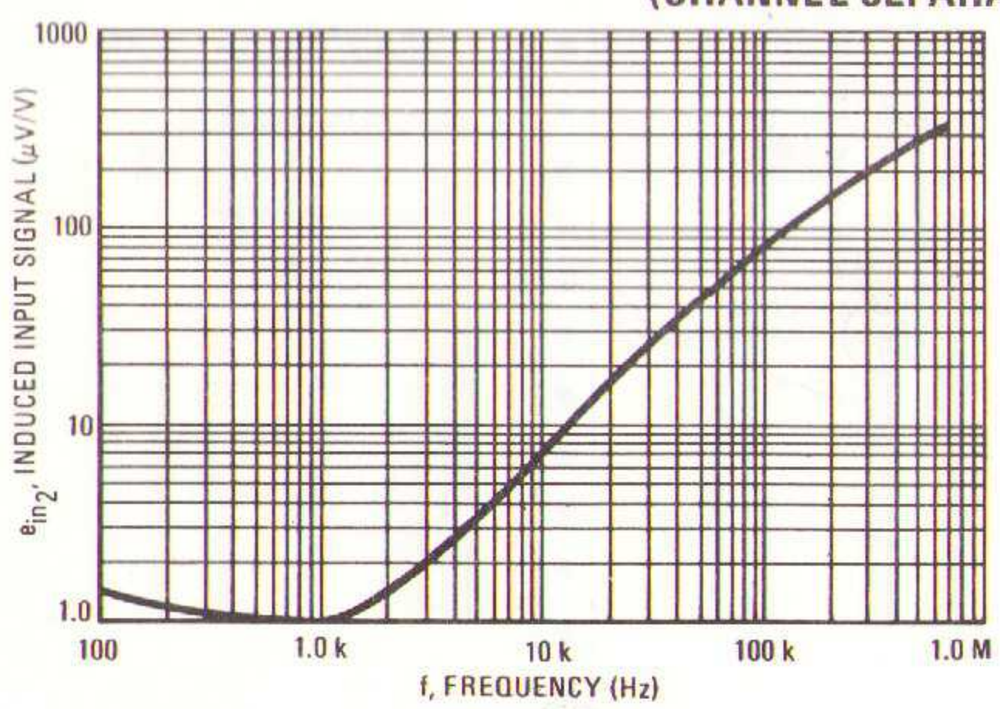
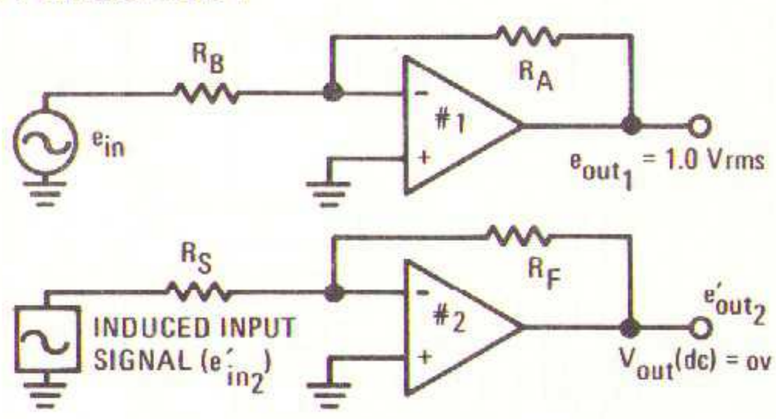


FIGURE 10 – INDUCED INPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced input signal (μV of induced input signal in amplifier #2 per volt of output signal at amplifier #1)

$e'_{out_2} = e'_{in_2} \times \frac{R_F}{R_S}$, where e'_{out_2} is the component of e_{out_2} due only to lack of perfect separation between the two amplifiers.

MOTOROLA Semiconductors

BOX 955 • PHOENIX, ARIZONA 85001

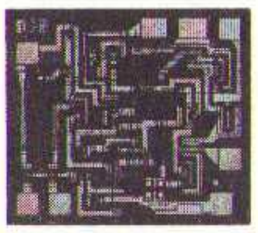
MC1709C

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

JUNE 1967 — DS 9070R1
(REPLACES DS 9070)

MONOLITHIC OPERATIONAL AMPLIFIER



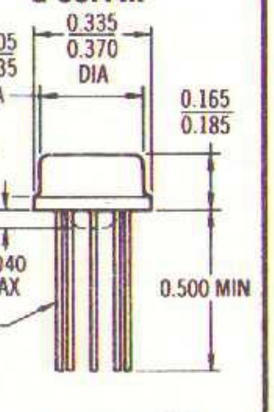
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

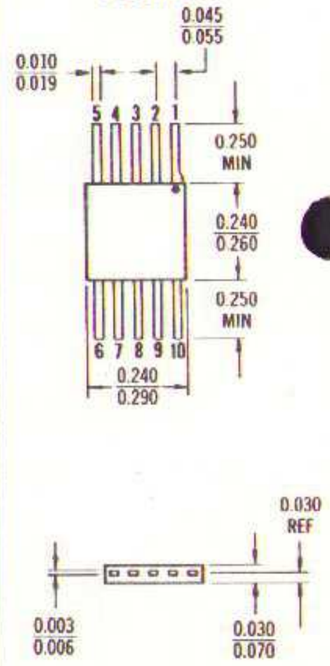
- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 45,000 typical
- Low Temperature Drift — ±3 μV/°C
- Large Output Voltage Swing —
  ±14 V typical @ ±15 V Supply
- Low Output Impedance — Z_{out} = 150 ohms typical

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±V^+	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	I_S	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C Plastic Package Derate above 25°C	P_D	 680 4.6 500 3.3 400 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range Metal Can and Flat Package Plastic Package	T_{stg}	 -65 to +150 -65 to +125	°C

* For full temperature range (-55°C to +125°C) and characteristic curves, see MC1709 data sheet.

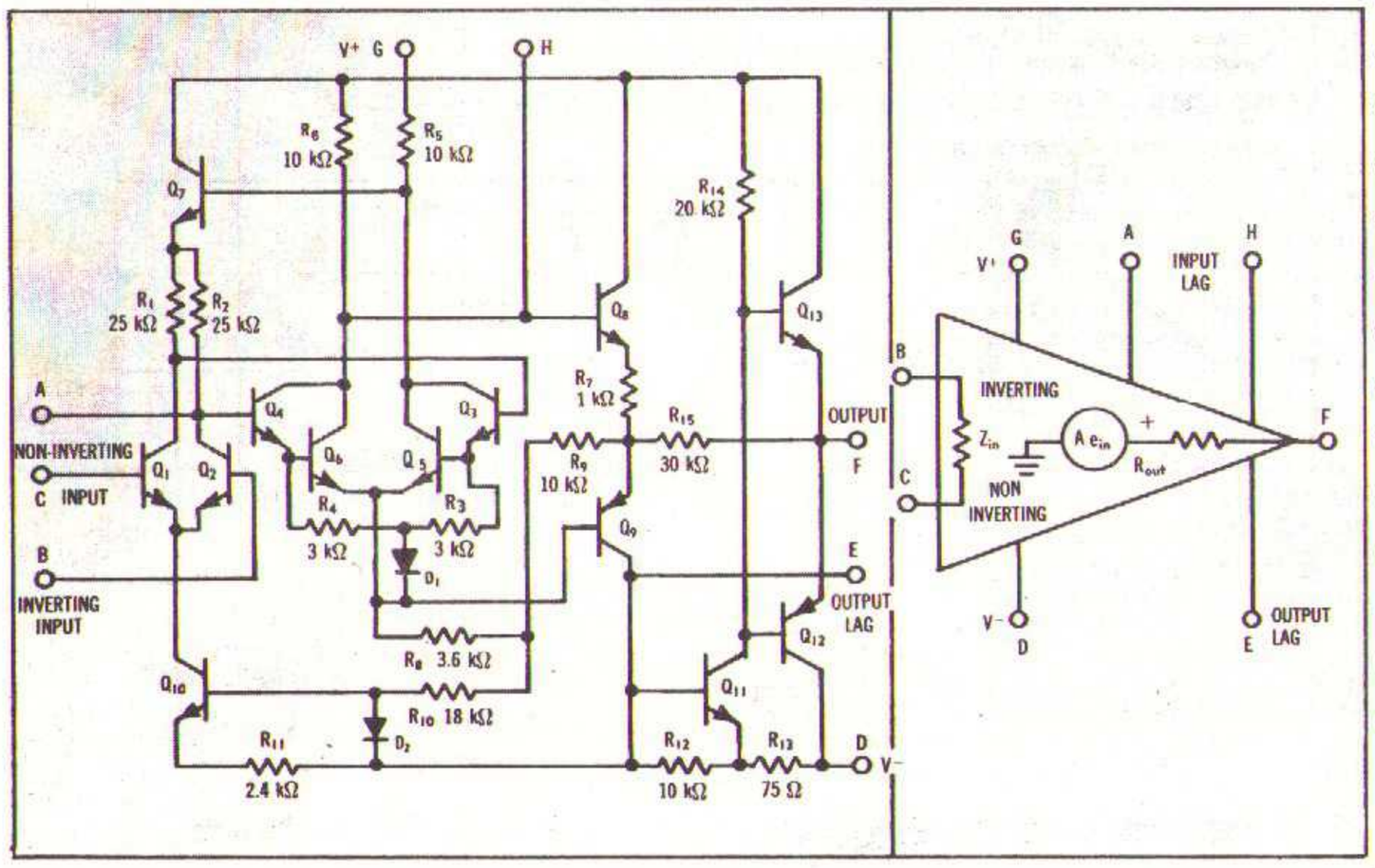


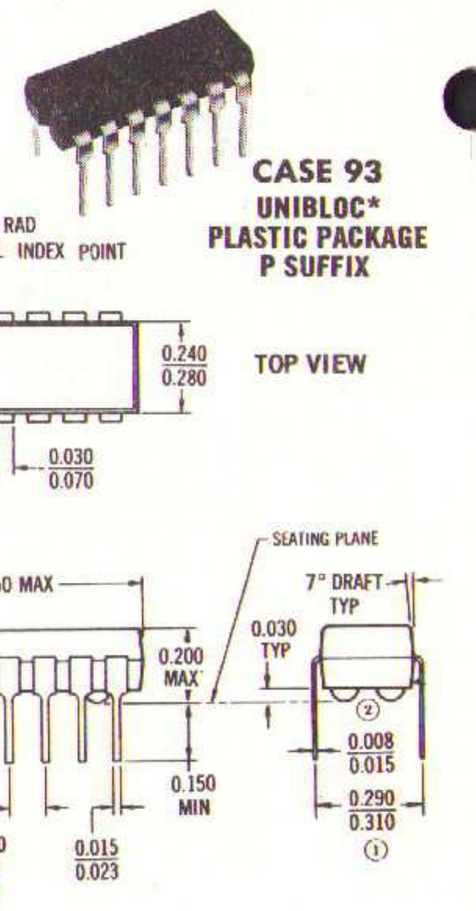


PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H
"G" Package	1	2	3	4	5	6	7	8
"F" Package	2	3	4	5	6	7	8	9
"P" Package	3	4	5	6*	9	10	11	12

*Pin 7 is electrically connected to substrate and V^-





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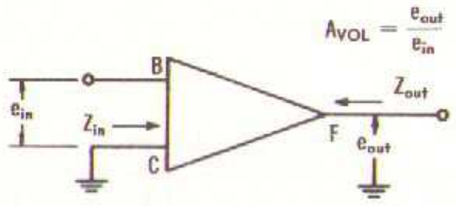
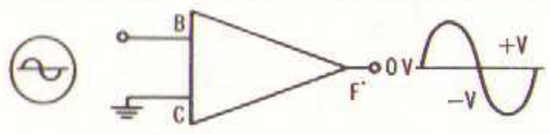
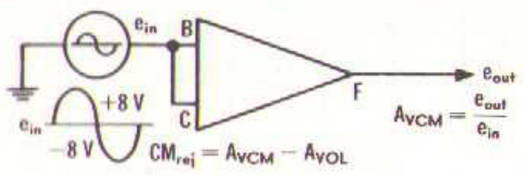
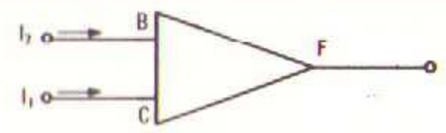
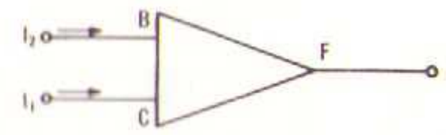
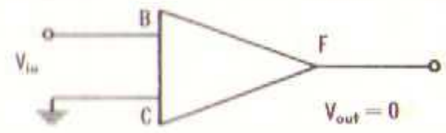
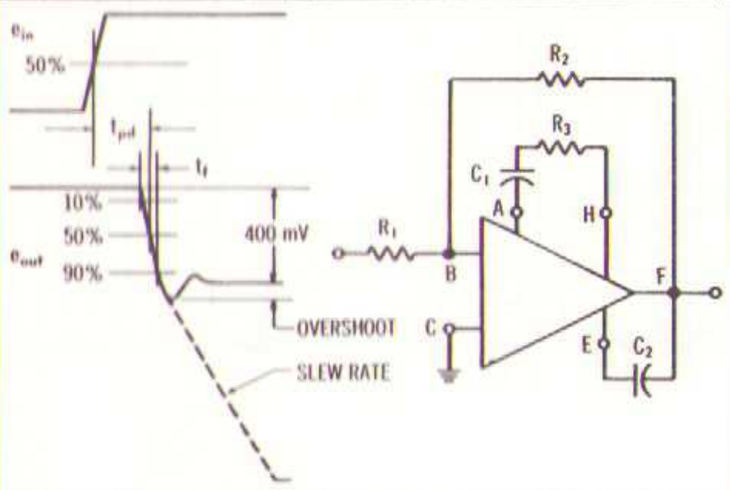
MC1709C

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (R_L=2 kΩ, V_{out} = ± 10 V, T_A = 0°C to +75°C)	A_{VOL}	15,000	45,000	-	-
	Output Impedance (f = 20 Hz)	Z_{out}	-	150	-	Ω
	Input Impedance (f = 20 Hz)	Z_{in}	50	250	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ) (R_L = 2 kΩ)	V_{out}	±12 ±10	±14 ±13	- -	V_{peak}
	Input Common Mode Voltage Swing	CMV_{in}	±8.0	±10	- -	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	65	90	-	dB
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$, ($T_A$ = +25°C) (T_A = 0°C)	I_b	- -	0.3 -	1.5 2.0	μA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, T_A = 0°C) ($I_{io} = I_1 - I_2$, T_A = +75°C)	I_{io}	- - -	0.1 - -	0.5 0.75 0.75	μA
	Input Offset Voltage (T_A = 25°C) (T_A = 0°C, +75°C)	V_{io}	- -	2.0 -	7.5 10	mV
	Step Response Gain = 100, 5% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3 pF	t_f t_{pd} dV_{out}/dt ①	- - -	0.8 0.38 12	- - -	μs μs V/μs
	Gain = 10, 10% overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF	t_f t_{pd} dV_{out}/dt ①	- - -	0.6 0.34 1.7	- - -	μs μs V/μs
	Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF	t_f t_{pd} dV_{out}/dt ①	- - -	2.2 1.3 0.25	- - -	μs μs V/μs
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = 0°C to +75°C) ($R_S \leq$ 10 kΩ, T_A = 0°C to +75°C)	TC_{Vio}	- -	3.0 6.0	- -	μV/°C
	DC Power Dissipation (Power Supply = ±15 V, V_{out} = 0)	P_D	-	80	200	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	25	200	μV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	25	200	μV/V

① dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 1 — TEST CIRCUIT
$V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25°C$

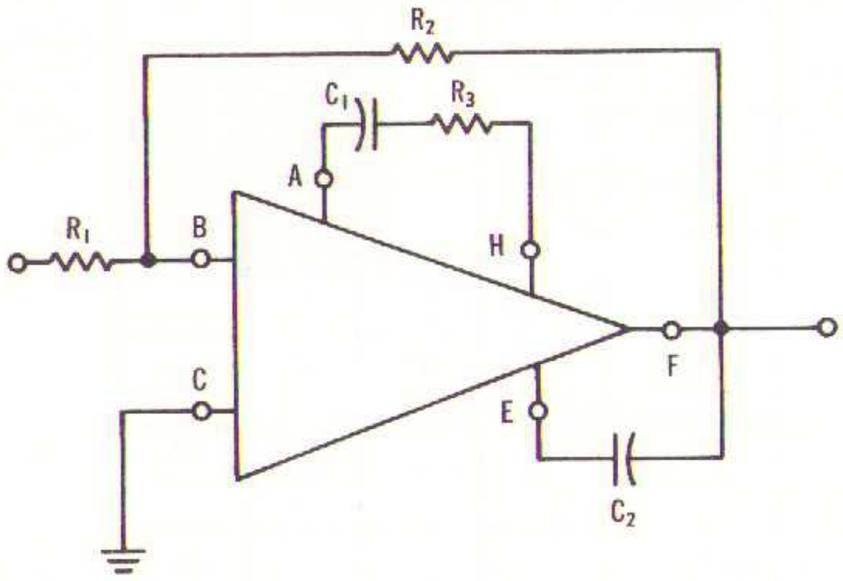


Fig. No.	Curve No.	Test Conditions				
		$R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	C_1(pF)	C_2(pF)
2	1	10 k	10 k	1.5 k	5 k	200
	2	10 k	100 k	1.5 k	500	20
	3	10 k	1M	1.5 k	100	3
	4	1 k	1M	0	10	3
3	1	1 k	1M	0	10	3
	2	10 k	1M	1.5 k	100	3
	3	10 k	100 k	1.5 k	500	20
	4	10 k	10 k	1.5 k	5 k	200
4	1	0	∞	1.5 k	5 k	200
	2	0	∞	1.5 k	500	20
	3	0	∞	1.5 k	100	3
	4	0	∞	0	10	3

FIGURE 2 — LARGE SIGNAL SWING versus FREQUENCY

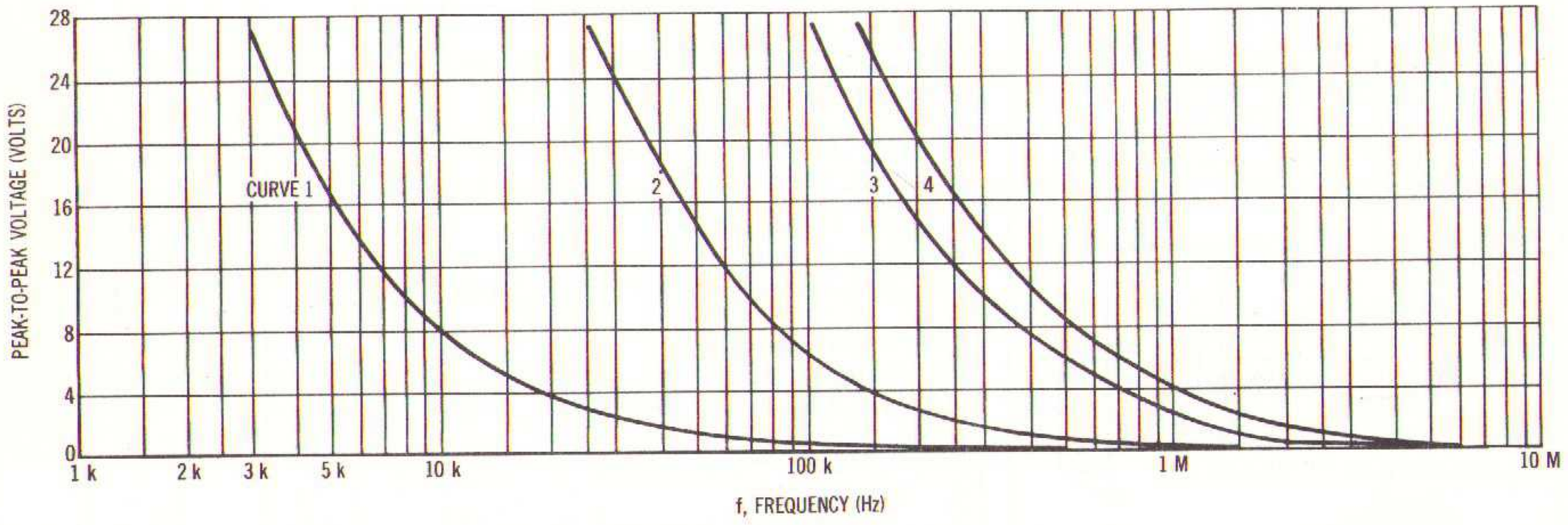


FIGURE 3 — VOLTAGE GAIN versus FREQUENCY

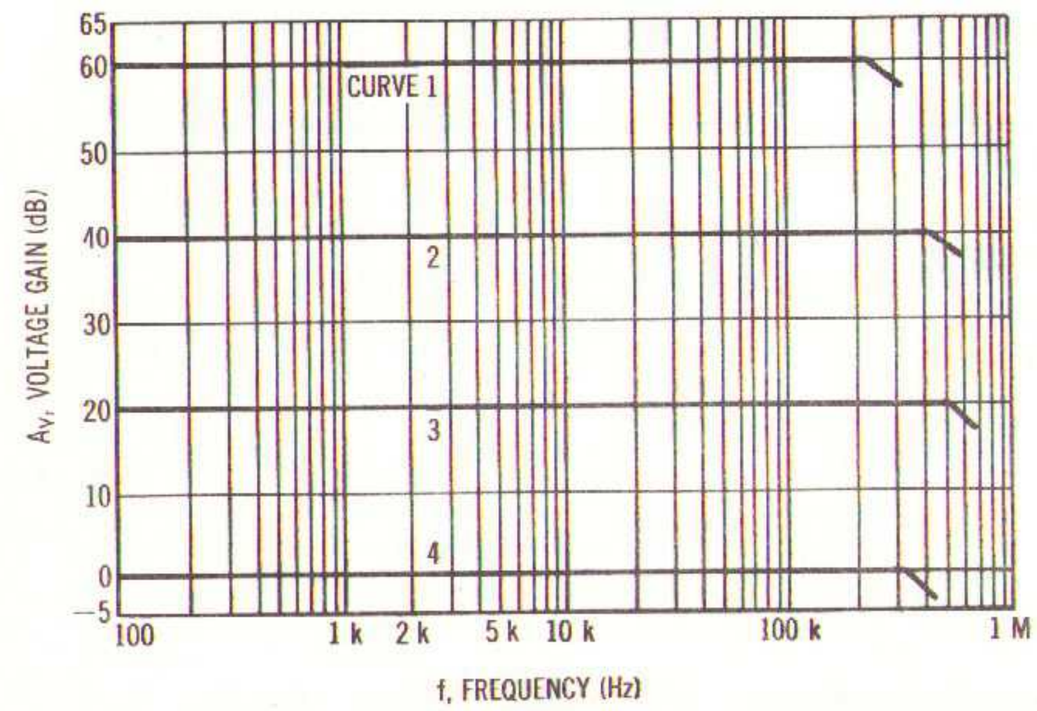


FIGURE 4 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY

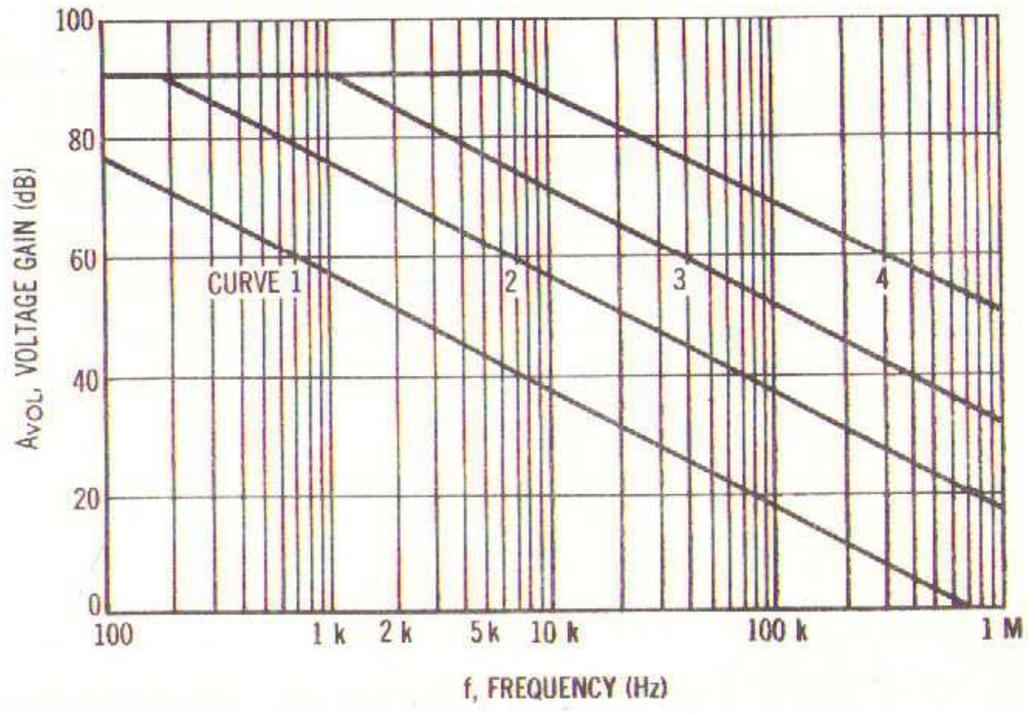


FIGURE 5 — POWER DISSIPATION versus POWER SUPPLY VOLTAGE

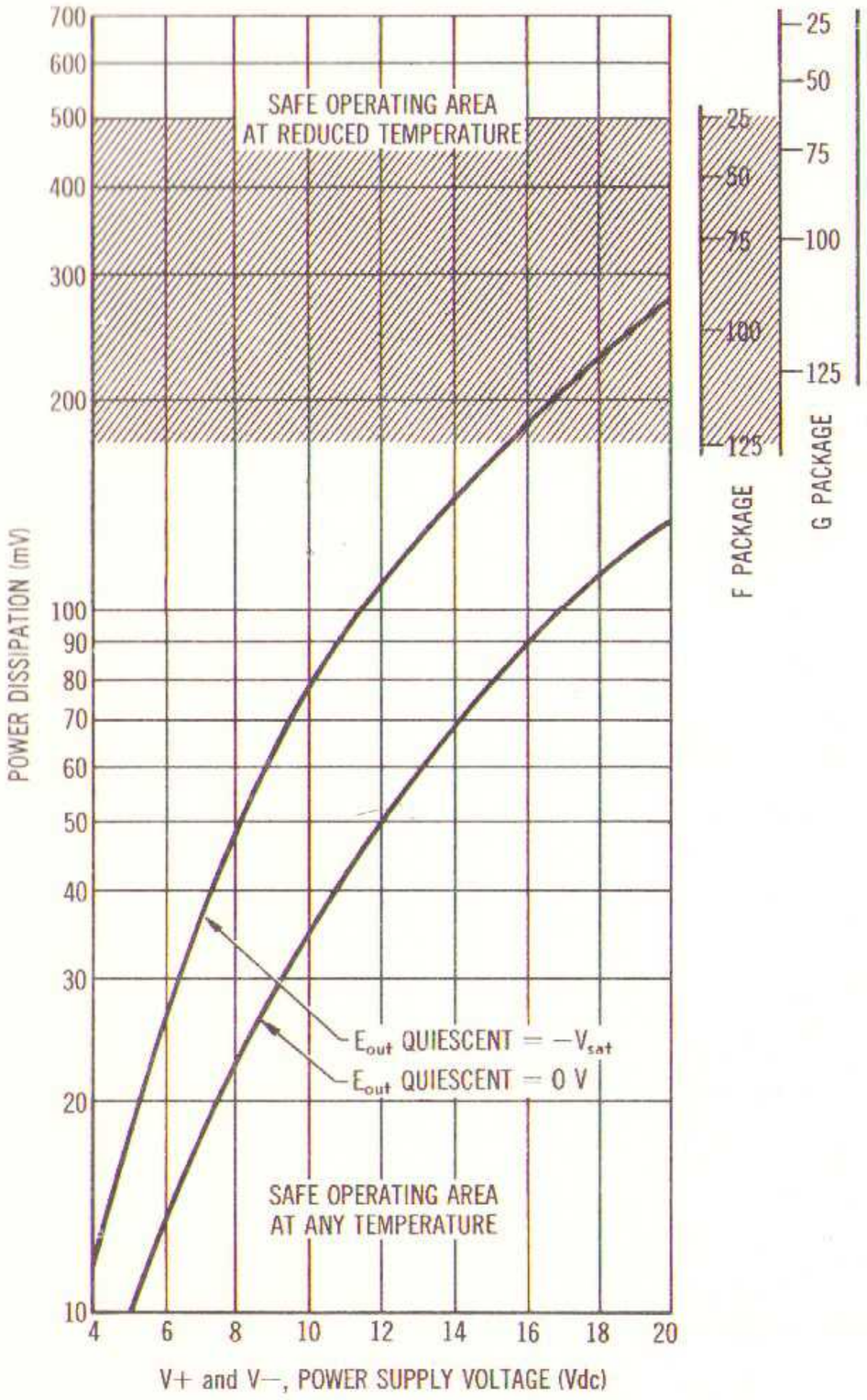


FIGURE 6 — VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

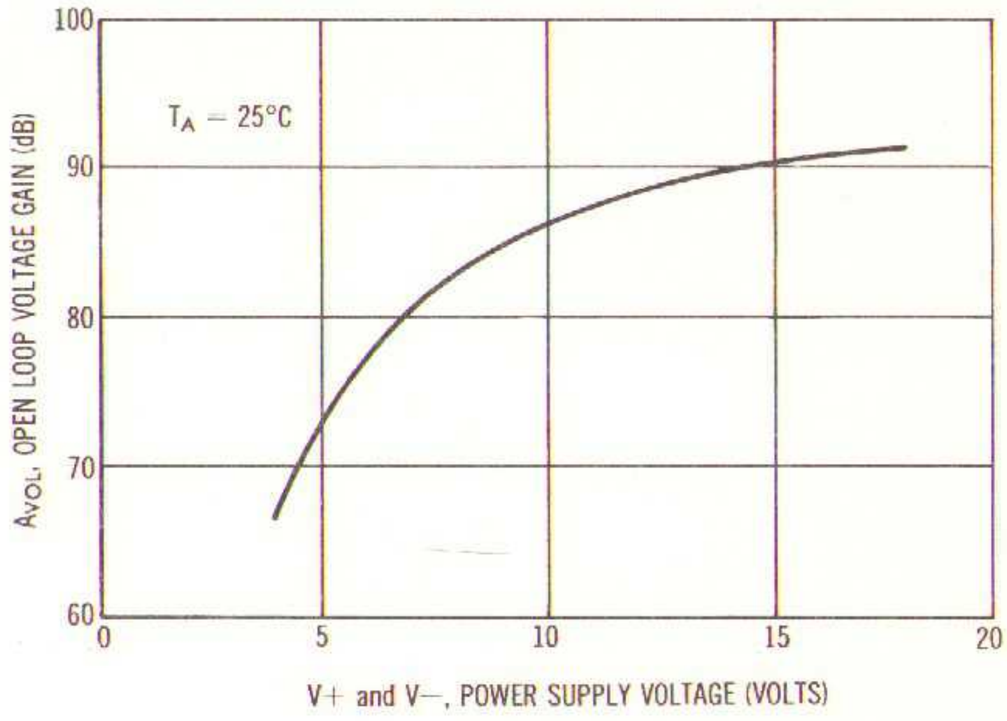


FIGURE 7 — [illegible] SWING versus POWER SUPPLY VOLTAGE

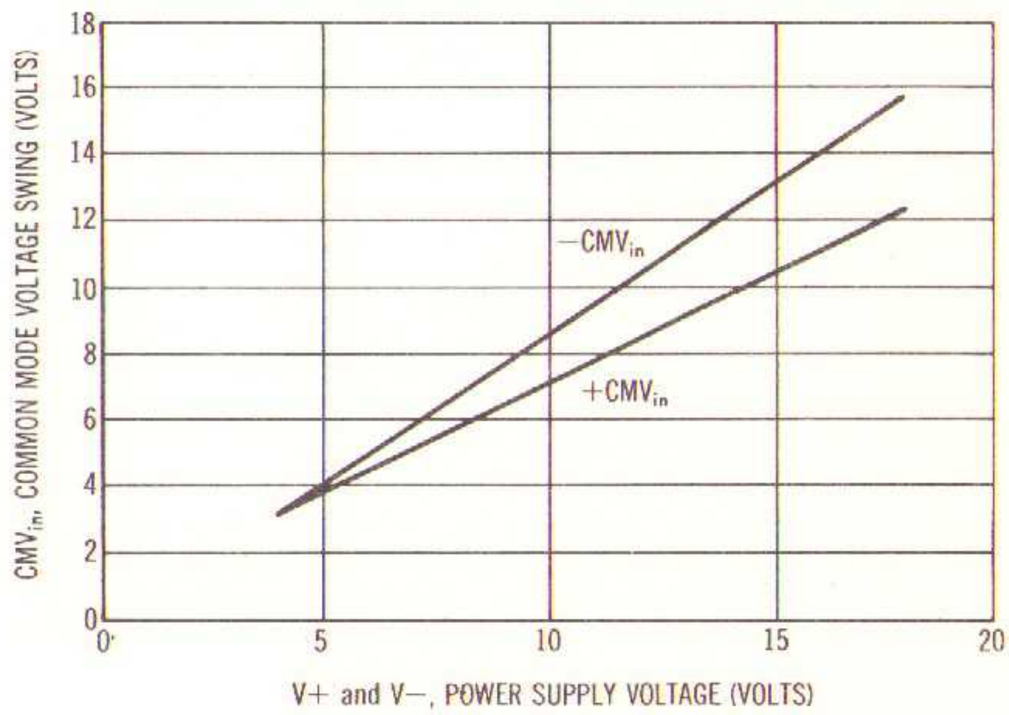


FIGURE 8 — INPUT OFFSET VOLTAGE versus TEMPERATURE

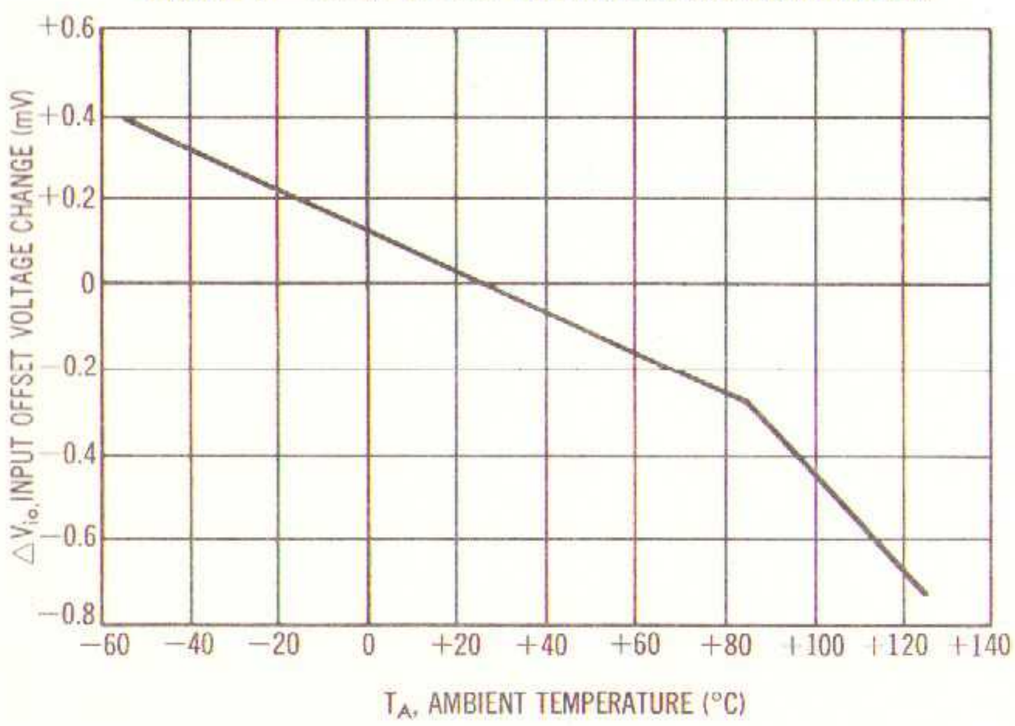
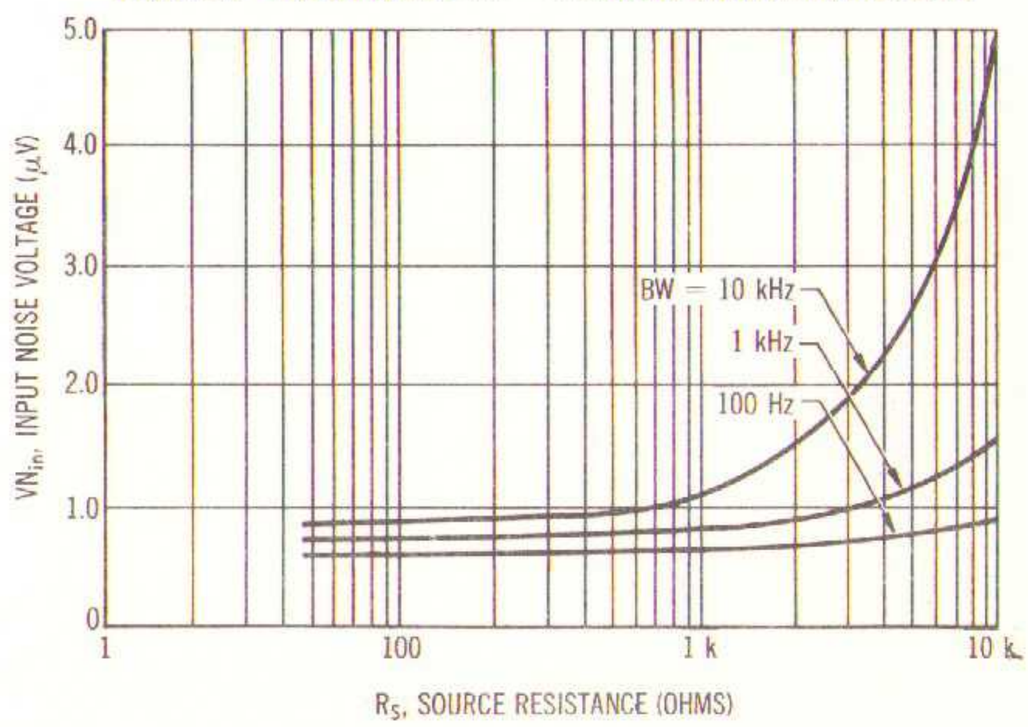


FIGURE 9 — INPUT NOISE [illegible] versus SOURCE RESISTANCE



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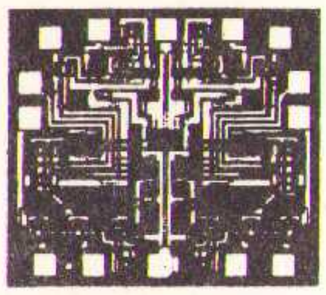

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W I J Z I J N O P M A A N D A G G E S L O T E N ! ! ! ! ! ! !

Prijzen van de genoemde componenten:

2C415 (dual NPN transistor)	f 7,75
2N4905 (PNP, complementair met de 2N4914)	f 24,75
2N4914 (NPN, complementair met de 2N4905)	f 15,50
2N3789 (PNP, complementair met de 2N3713)	f 46,75
2N3713 (NPN, complementair met de 2N3789)	f 23,00
108T2 (NPN power 175 watt)	f 59,50
109T2 (NPN power 175 watt)	f 62,50
CA 3000 (Differentiaal versterker met constante stroombron)	f 23,50
CA 3012 (Opgenomen in Technische Documentatie deel 2, blz. 14-19)	f 10,50
CA 3018 (Darlington transistor met 2 x NPN)	f 12,25
CA 3020 (Audio versterker)	f 14,50
CA 3028 (Breedband differentiaal versterker met stroombron)	f 8,00
MC 1430 (Operationele versterker tot ruim 10 MHz)	f 27,15
MC 1435 (Dubbele operationele versterker tot 10 MHz)	f 39,50
MC 1709 (≙ µA 709, RE709, TOA 709) operationele versterker	f 10,00
SN72709BN (zie T.D. 1969 deel 3 blz. 9; speciale µA 709)	f 9,00
MC 1439 (Oversturings- en kortsluitvaste uitvoering MC 1709)	f 15,50

Voor verscheidene van bovenstaande geïntegreerde schakelingen is een speciale prijsnotering bij afname van 10, 25, 100, 250 en 500 stuks van toepassing; onze verkoopafdeling zal U hierover nader kunnen informeren.

Voor bovenstaande produkten worden ook diverse soorten montagematerialen geleverd, o.a. insteekvoeten. Voor een overzicht van de leverbare voeten verwijzen wij U naar Technische Documentatie 1969 deel 5-6 blz. 36.

Alle prijzen zijn incl. 12% B.T.W.; prijswijzigingen strikt voorbehouden.

In ons leveringsprogramma zijn ook opgenomen:

= onderdelenpakketten voor audio versterkers van 3 watt tot 90 watt.
= onderdelenpakketten voor digitale apparaten.
= connectors, IC-voeten, duimwielschakelaars, printplaten, enz.
= onderdelenpakketten voor elektronische circuits in auto's (o.a. intervalschakeling voor ruitenwisser en thyristor-ontstekingen.
= weerstanden (kool en metaalfilm), condensatoren (metaal papier, polyester), elco's fabr. Rifa.
= keramische condensatoren.
= montagekasten en montagematerialen.
= pluggen, chassisdelen, knoppen, schakelaars, indicatielampjes, montagedraad, wikkeldraad, koelplaten, isolatiematerialen, enz.
= universeelmeters en paneelmeters fabr. Hansen.
= circa 100 verschillende technische boeken over vele onderwerpen.
= luidsprekers van o.a. Audax, Kef, Philips, Isophon.
= gemonteerde en afgeregelde FM bouwstenen fabr. Görler.
= transistoren, thyristoren, triacs, fets, dioden, zenerdioden, bruggelijkrichters, geïntegreerde schakelingen, UJT's, tunneldioden, triggerdioden, enz. van bekende fabrikanten als I.T.T., Texas Instruments, R.C.A., Motorola, Semicron, Philips, Siemens, enz.